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Etude, modélisation et optimisation des dispositifs de puissance :
Application à la commande des systèmes photovoltaïques

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Dedication

To my parents and all the greats who have inspired me, I dedicate this modest work.

Abstract

Power semiconductor devices are an important part of the technological revolution of the second half of the 20th century as they are the basis of the modern conversion of the electric power. Since the last two decades, new market of power devices has evolved in response to the requirements of emerging technologies such as electric vehicles, hybrid electric vehicles, and renewable energies in general. In such areas, demands of increasing reliability and efficiency are continually growing. In order to fulfill those demands, the scientific community is urged to keep advancing in the design, modeling, and optimization of power devices.

The work accomplished in this dissertation was established within this framework of design, modeling, and optimization of power devices, where new approaches of power devices design have been developed and exploited successfully. Precisely, a new approach of junctionless (JL) power devices have been proposed and utilized in power MOSFETs. As a result, two novel power MOSFETs designs have been presented, namely a junctionless planar power MOSFET, and a junctionless trench power MOSFET. Those two devices encompasses improvements related to the physics underlying the functioning of power MOSFETs.

Numerical modeling and investigation of the combination of the JL concepts with the planar and trench power MOSFETs have been carried out and presented in this dissertation, and improvements regarding the breakdown capability, the on-resistance, the threshold voltage, the switching speed, and the switching losses have been demonstrated in comparison to high-performance recently published power devices. The analysis of the performance of the JL trench power MOSFET on a circuit level analysis based on the boost DC-DC converter mode of operation is performed, and the results proves the superiority of our proposed device in comparison to its conventional counterpart, which discloses a high performance regarding boost mode operation in DC-DC converters for the control of photovoltaic panels.

Key words: Power MOSFET, Junctionless MOSFET, SiC MOSFET, Numerical simulation, power devices optimization, photovoltaic control.

Résumé

Les dispositifs à base de semi-conducteurs de puissance constituent une partie importante de la révolution technologique de la seconde moitié du XXe siècle, car ils constituent la base de la conversion moderne de l'énergie électrique. Depuis les deux dernières décennies, de nouveaux marchés de dispositifs électriques ont évolué en réponse aux exigences des technologies émergentes telles que les véhicules électriques, les véhicules électriques hybrides et les énergies renouvelables en général. Dans ces domaines, les exigences en matière de fiabilité et d'efficacité ne cessent de croître. Afin de répondre à ces demandes, la communauté scientifique est invitée à continuer de progresser dans la conception, la modélisation et l'optimisation des dispositifs électriques de puissance.

Le travail accompli dans cette thèse s'inscrit dans ce cadre de conception, de modélisation et d'optimisation de dispositifs de puissance, où de nouvelles approches de conception de dispositifs de puissance ont été développées et exploitées avec succès. Plus précisément, une nouvelle approche de dispositifs de puissance sans jonction (JL) a été proposée et utilisée dans les MOSFET de puissance. En conséquence, deux nouvelles structures de MOSFET de puissance ont été présentées, à savoir un MOSFET de puissance planaire sans jonction et un MOSFET de puissance trench gate sans jonction. Ces deux dispositifs englobent des améliorations liées à la physique gouvernant le fonctionnement des MOSFET de puissance.

La modélisation numérique et l'étude de la combinaison des concepts JL avec les MOSFET de puissance planaire et trench gate ont été réalisées et présentées dans cette thèse, ainsi que des améliorations concernant la tension de claquage, la résistance de l'état ON, la tension de seuil, la vitesse de commutation et les pertes de commutation ont été démontrées par rapport aux dispositifs de puissance à hautes performances récemment publiés. L'analyse des performances du MOSFET de puissance proposé en un circuit de puissance proche du principe de fonctionnement des convertisseurs boost DC-DC est effectuée et les résultats prouvent la supériorité du dispositif proposé par rapport à son homologue conventionnel, qui révèle une haute performance en termes de fonctionnement en mode boost dans les convertisseurs DC-DC pour la commande des panneaux photovoltaïques.

Mots clés : MOSFET de puissance, MOSFET sans jonction, SiC MOSFET, simulation numérique, optimisation des dispositifs de puissance, commande des panneaux photovoltaïques.

ملخص

تعد الأجهزة المطورة من أشباه النواقل ذات الاستطاعة جزءًا مهمًا من الثورة التقانية في النصف الثاني من القرن العشرين، لأنها أساس بنى التحويل الحديثة للطاقة الكهربائية. ومنذ العقدين الأخيرين، شهدت سوق الأجهزة ذات الاستطاعة نموا كبيرا وآفاقا جديدة استجابة لمتطلبات التقنيات الناشئة مثل السيارات الكهربائية، والمركبات الكهربائية الهجينة، والطاقات المتجددة بشكل عام. وفي مثل هذه المجالات، تتزايد باستمرار متطلبات الموثوقية والكفاءة المتعلقة بالأجهزة. ومن أجل تلبية هذه المطالب، فإن المجتمع العلمي يعمل باجتهاد لمواصلة التقدم في تصور الأجهزة ذات الاستطاعة ونمذجتها وتصميمها وتحسينها.

إن العمل المنجز في هذه الأطروحة يدخل ضمن هذا الإطار المتعلق بتصور الأجهزة ذات الاستطاعة ونمذجتها وتصميمها وتحسينها، وقد أثمر هذا الجهد تطويرا لأساليب جديدة في تصميم الأجهزة ذات الاستطاعة. وبوضوح أكثر، فإننا اقترحنا نهجا جديدا للأجهزة ذات الاستطاعة عديمة الفجوات (JL) واستخدامها في المقحلات (MOSFETs) ذات الاستطاعة. ونتيجة لذلك، أصدرنا تصميمين جديدين لوحدات MOSFET ذات الاستطاعة، وهما مقحل مسطح عديم فجوات، ومقحل مثلوم عديم فجوات. ويشتمل هذان الجهازان على تحسينات عميقة تنبع من المبادئ الفيزيائية لعمل المقحلات ذات الاستطاعة.

وفي هذا السياق، أجرينا نمذجة عددية متعقلة بالمزاوجة بين مبدأ انعدام الفجوات والبنية المثلومة للمقحلات ذات الاستطاعة ثم أتبعناها بتحليل للنتائج وعرض لها في هذه الأطروحة، وقد أظهرت نجاعة عالية متعلقة بتوتر الانهيار، والمقاومة أثناء التوصيل، وتوتر العتبة، وسرعة التبديل، وفقدان الطاقة أثناء التبديل بالمقارنة مع أجهزة عالية الأداء منشورة مؤخرًا. أخيرا، أجرينا تحليل أداء للمقحل ذي الاستطاعة المقترح في دارة ذات استطاعة شبيهة في وظيفتها لمبدأ عمل محول التعزيز DC-DC، وأثبتت النتائج تفوق هذا الجهاز المقترح مقارنة بنظيره التقليدي، وهذا يظهر الأداء العالي للجهاز فيما يتعلق بتشغيل وضع التعزيز في المحولات DC-DC للتحكم بالصفائح الكهروضوئية.

كلمات جامعة: مقحل ذو استطاعة، مقحل عديم الفجوة، مقحل السيلكون الكربوني، نمذجة عددية، تحسين الأجهزة ذات الاستطاعة، التحكم في الصفائح الكهروضوئية.

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General introduction

Introduction and motivation

From the simple welding machine and the first SiC-based Schottky diode 20 years ago, devices based on wide bandgap materials have continue to evolve over the course of years until now. Actually, between 2018 and 2023, exclusively three materials dominated the market of power devices: silicon, silicon carbide, and gallium nitride. In 2018, the worldwide power semiconductor devices market was estimated at $17.5 billion shared between several discrete power devices. However, in 2024, the same market is expected to reach $22 billion, making a growth of $750 million per year. In fact, SiC-based devices have a market share of about 16 % in 2024 compared to 6 % in 2018, thanks to emerging EV and hybrid EV market including charging stations and energy storage equipment, together with renewable energy market, a growth that is believed to continue increasing in the future. In that sector, decreasing the size and weight with enhancing the efficiency is of the first importance [1-3].

At the early stages of the semiconductor industry, silicon was believed to be capable of doing anything in the domain of semiconductor devices. One aspect of that is the ongoing dominance of silicon utilization in power devices, which could be seen in the market share of those devices estimated at 76 % in 2024. However, this dominance will not continue in the forthcoming years due to the exhaustion of all silicon properties at their theoretical limits, figuratively, we can say that silicon is driven by its brilliant past, not its promising future. As such, high demands of ruggedness, increasing power density, and elevating blocking voltages, with high efficiency are out of the silicon span [4-5]. As those industrial requirements could not be fulfilled without wide bandgap materials, their market share grows with the spreading of new power applications based on those requirements in our daily life.

In that context, the scientific research on this field is focusing on bringing in new innovative solutions, which overcome problems using wide bandgap materials [1-6]. While the industrial mass production and the mature technology in power electronics is restricted to silicon, silicon carbide, and III-nitrides, the scientific research scope is far beyond those three materials. For instance, the most recent material with the lowest maturity gallium oxide (Ga_2O_3) is gaining attention in serious scientific research circles, where too much effort has to be made for years running and maybe decades, before this material establish itself in the industry [1].

Practically, Si-IGBT is still a dominant power device in the market for high voltage and low frequency applications, with a market share of about 30 %. However, advances in silicon carbide

technology during the past two decades is translated into a SiC-MOSFET that is by far capable of surpassing Si-IGBT in terms of switching losses, switching frequency, ruggedness, as well as power density, and miniaturization, provided that the SiC-MOSFET use is affordable, because SiC technology is still very expensive compared to silicon technology. In fact, available SiC-MOSFETs could reach 500 kHz with 98.5 % efficiency for an output current around 16 A [7]. Nevertheless, SiC-MOSFET is still far below its theoretical limits, mainly due to SiC/SiO_2 interface poor quality causing threshold instabilities, and affecting the channel mobility, which increases the ON resistance. As a result, the device performances are compromised [7-8].

Motivated by both SiC-MOSFET constraints, the high fabrication cost, and the poor SiC/SiO_2 interface quality, we have aimed at reducing the intensity of these problems by means of a new methodology with respect to power devices. In fact, common solutions deal with the improvement of the growth process, which is effective but expensive and complicated [9-11]. Furthermore, less effective and less expensive simple solutions try with the insertion of electric field modulating layers, such as P-type buried layers, shielded regions, floating islands, or buried oxides.

In this sense, we have realized that our work has to be initiated from the conception level moving to the modeling level through a radical approach with new SiC-MOSFET structures, which combine simplicity with effectiveness and low cost, consolidated by a validation of their high performances via comparison with recently published works, and conventional cases. A thorough analysis has led us to the junctionless approach, which eliminates the inversion layer instead of trying to improve it. From a physical point of view, we have tried to propose a device, which has the ability to carry a volume current under the gate instead of the sheet current resulting from the inversion layer in all conventional power MOSFETs with pn junctions. Such solution would be beneficial for the mobility, because it would be a mobility of majority carriers instead of a mobility of inversion carriers. Furthermore, in such case we would be successful in reducing the hindering effects of the SiC/SiO2 interface by giving the charge carriers another dimension to stay away from the interface or at least circumvent the close contact with it. Most importantly, the elaboration of this solution relieves the budget of the very expensive enhancement of the SiC/SiO2 by growth processes, and surprisingly, it is less expensive than the elaboration of a conventional pn junction power MOSFET.

This approach has yielded novel high-performance cost-effective power devices when compared with their conventional counterparts for power electronics applications [12-13].

Layout of the dissertation

The research content of our work is structured as a dissertation in the form of four chapters. The first chapter deals with the wide bandgap materials properties and applications in power electronics, where we present the material employed in our work, which is a basis towards the design of the device. At first, we discuss its crystal structure, from which stem all the material properties. Subsequently, in the light of the crystal properties, we provide an overview on the electrical properties, alongside a brief discussion of the SiC/SiO_2 interface, as they determine any SiC device performances. For the sake of comparison, the industrial and market rivals of silicon carbide are described and presented, namely the group of III-nitrides. Followed by an outline of gallium oxide, which is one of the newest and promising wide bandgap materials. Afterwards, we provide a brief description of the three most important power devices based on silicon, SiC, and GaN. Finally, power converters based on power devices are discussed and comparisons are performed with respect to silicon-based power devices.

In the second chapter, our attention is focused on the development and the numerical analysis of the first structure using the junctionless concept. The device, which is a novel junctionless planar power MOSFET, is presented and the key ideas behind its architecture are given.

Furthermore, the semiconducting behavior and the electrical properties of the new device are validated by comparison with the conventional counterpart not only that, but also the device superior figure of merit is shown and compared with recently published high-performance devices. This structure is certainly simple in terms of fabrication, as it shortcuts many steps of the fabrication of devices with p-n junctions, and it shows higher performance demonstrated by its superior figure of merit.

In the third chapter, we push forward our established junctionless concept to adapt it with the trench gate structure, as a result, a masterpiece novel junctionless trench power MOSFET is developed and its structure is explained. Following that, we carry out a numerical investigation of its switching characteristics, then, its forward and blocking properties. Moreover, we provide a numerical validation of its semiconducting behavior. This device shows an outstanding switching figure of merit and blocking figure of merit proved by comparison with recently published high performance devices, in addition to its inherent low cost of fabrication.

The forth chapter is divided into two parts, the first part is dedicated to the problem of the quasi-saturation in power MOSFETs since it represents a degradation of the device performance when

it is subject to high gate voltages. Besides, an alleviating strategy is proposed and the associated improvements are shown. The second part is devoted to a circuit level analysis of our proposed trench SiC-MOSFET with its conventional counterpart. On this level, the switching performances of our device and its conventional counterpart are analyzed in a circuitry related to a resistive load, then related to an inductive load. The main goal of this analysis is to show suggestions of the effectiveness of our proposed device use in DC-DC power converters related to photovoltaic panels, and open up the door towards more in-depth circuit level analysis.

Finally, general conclusions about our accomplished work along this dissertation are given and future prospects regarding the implementation of our proposed device in power electronics and further research guidelines are presented.

References

[1] Fan Ren, Stephen J Pearton. Wide bandgap semiconductor-based electronics. IOP publishing, 2020.

[2] B. Jayant Baliga. Silicon carbide power devices: progress and future outlook. IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, pp. 2400-2411, 2023.

[3] H Ferhati, F Djeffal, N. Boubiche, F. Le-Normand, An efficient ITO-free transparent electrode based on diamond-like carbon with an engineered intermediate metallic thin-film, Solar Energy, Vol. 196, Pages 327-335, 2020.

[4] F. Djeffal, D.Arar, Z. Dibi, N. Lakhdar, An approach based on particle swarm computation to study the electron mobility in wurtzite GaN, Symposium on Wide band gap semiconductor nanostructures for optoelectronic applications E-MRS 2008, May 26-30, 2008, Strasbourg, France.

[5] Omar Sarwar Chaudhary, Moloud Denai, Shady S. Refaat. Technology and Applications of Wide Bandgap Semiconductor Materials: Current State and Future Trends. Energies, 16(18):6689, 2023.

[6] Matteo Meneghini, Srabanti Chowdhury, Joff Derluyn, Farid Medjdoub. Springer Handbook of Semiconductor Devices. Springer press, 2022.

[7] Yasin Gunayadin, Saeed Jahdi, Olayiwola Alatise, Jose Ortiz Gonzalez, et al. Performance of Wide-Bandgap discrete and module cascades at sub-1kV: GaN vs. SiC. Microelectronics reliability, vol. 125, 114362, 2021.

[8] Y. Hu, J. Shao and T. S. Ong. Application of SiC MOSFETs in 6.6 kW High-Frequency High-Power-Density Power Converter. PCIM Europe digital days 2020; International exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy, Germany, pp. 1-5, 2020.

[9] Ferhati, H., Djeffal, F., Bendjerad, A., Saidi, A., & Benhaya, A. Post-annealing effects on RF sputtered all-amorphous ZnO/SiC heterostructure for solar-blind highly-detective and ultralow dark-noise UV photodetector. Journal of Non-Crystalline Solids, 574, 121168, 2021.

[10] Benyahia, K., Djeffal, F., Ferhati, H., Benhaya, A., Bendjerad, A., Djaballah, Y., & Martin, N. Microstructured ZnO-ZnS composite for earth-abundant photovoltaics: Elaboration, surface analysis and enhanced optical performances. Solar Energy, 218, 312-319, 2021.

[11] Ferhati, H., Djeffal, F., Bendjerad, A., Foughali, L., Benhaya, A., & Saidi, A. Highly-detective tunable band-selective photodetector based on RF sputtered amorphous SiC thin-film: Effect of sputtering power. Journal of Alloys and Compounds, 907, 164464, 2022.

[12] B. Zerroumda, F. Djeffal, S. Benaggoune, H. Ferhati. Performance assessment of a novel 4H–SiC junctionless planar power MOSFET towards improving electrical properties. Micro and Nanostructures, vol. 169, pp. 207346, 2022.

[13] B Zerroumda, H Ferhati, F Djeffal, S Benaggoune. A novel high-performance junctionless 4H-SiC trench MOSFET with improved switching characteristics. Microelectronic Engineering, vol. 277, pp. 112011, 2023.

Chapter I

Wide bandgap materials and related power electronics

1.1 Introduction

Wide bandgap technology is relatively a 21st century developed domain, which encompasses various compound materials such as silicon carbides (4H-SiC, 6H-SiC, 3C-SiC), the nitrides (GaN, AlN, InN, BN …), diamond (C), gallium oxide (Ga_2O_3), zinc oxide (ZnO) … etc. Generally, the decisive way of choosing between wide bandgap materials is the right technology for the right type of application, i.e. each material has its specific domain where it provides the best attainable compromise. However, due to several technological challenges, only two set of materials have an established industrial market, namely SiC and III-nitrides. From a technological point of view, SiC has the advantage of similarity with silicon over all wide bandgap materials, in a way that all technologies applicable to silicon can be translated to silicon carbide [1-5].

Generally, at low voltage and low frequency, silicon is still the dominant material in commercially available power devices, by virtue of its low cost [6]. In the meanwhile, silicon undergoes a continuous replacement as a power material by prominent wide bandgap technologies due to its high switching losses, low critical electric field and low switching frequencies. Actually, at low voltage and high frequency GaN is the material of choice in nowadays power industry. For instance, at 50 V GaN is less likely to breakdown due to high frequency switching, while maintaining a high mobility, so the manufacturer does not have to overdesign when targeting radio frequencies. Moreover, GaN is preferred over silicon when high power density is needed, which means less space is required for the same amount of power, for example in computer and phone chargers. Clearly, GaN-based light emitting diodes (LEDs) are widely used in our daily life as in flashlight of smartphones, electric lamps, and flat screens [7].

At high voltage (typically around 1 kV and higher) Silicon carbide exceeds by far GaN. In fact, from 600 V up to 1 kV there is only a slight increase in the on-resistance of silicon carbide devices, which means a better agreement between the breakdown voltage and the on-resistance could be achieved compared to GaN devices. Practically, for lateral integrated power devices, the limit of GaN in terms of voltage is around 600 V, beyond that limit the drain-source distance has to be increased significantly to prevent breakdown, which results in a drastic rise of the lateral GaN devices on-resistance, unless the device is designed vertically. In terms of power, GaN is used in applications in the range of hundreds of Watts. Beyond 1 kW, silicon carbide starts to regain the lead. Furthermore, silicon carbide is the favorite material in areas where the need for power grows

rapidly. In such case, power supplies outputs have to be adaptable allowing power modules to match a wide range of power demand. In fact, the most important feature of silicon carbide devices over gallium nitride devices is their ruggedness, which allows us a low safety margin for voltage in silicon carbide devices. Owing to this feature, Silicon carbide is notoriously the material to use in butteries intended for electrical vehicles. In addition, power grids are another thriving domain of silicon carbide, where SiC-based power devices control the electric power flow, in particular, SiC-MOSFETs and SiC-IGBTs arranged in power modules denoted as flexible AC transmission systems (FACTS) [8-11].

Given that the main scope of wide bandgap scientific research is on SiC with III-nitrides, and modern-day mature power technology is only SiC technology and to a lesser extent III-nitrides technology. Furthermore, in terms of mass production we find solely SiC and III-nitrides with established place in the market. In addition, cost-effective power devices are engineered based on either SiC or to a lesser extent III-nitrides, and most importantly, because the contribution of this work is carried out using SiC. An Important part of this chapter will be dedicated to the basic characteristics of those materials, with special focus on silicon carbide.

1.2 Silicon carbide

Among all wide bandgap materials silicon carbide is the wide spread adopted material in the industry, and so far, significant achievements have been made in the last decade to bring silicon carbide processing technology into maturity. Furthermore, silicon carbide is provided with outstanding high thermal conductivity, high critical electric field, interesting thermal stability of the on-resistance, and good chemical inertness, making it a promising material for next generation power devices [12].

1.2.1 Crystallographic structure of SiC

Silicon carbide crystal structure is built-up on a basis of covalently bounded atoms organized such that one atom of carbon at a tetrahedron center is covalently bounded to four adjacent silicon atoms at the summits of the same tetrahedron and vice versa, forming all together a tetrahedron. The length of the Silicon-Carbon bound is around 0.189 nm. In general, semiconductors at the molecular level form covalent bonds. Since, silicon and carbon are group IV materials in the periodic table, they normally form covalent bounds, with four shared outer electrons from each

atom, building a stable electronic outer shell of eight electrons. However, due to differences in electronegativity between silicon and carbon, an ionic part occurs and accounts for 11% of the bound. The tetrahedral structure of bounded atoms in the SiC lattice stems from the sp^3 hybridization that allows both carbon and silicon atoms to share four valence electrons to form covalent bounds. For all SiC polytypes, the tetrahedrons are linked to each other in a form of either wurtzite structure or zincblende structure. In both configurations, the distance between the basal plan containing three atoms of the same type and the top plan containing the summit atom is 0.252 nm. While the distance between the basal plane and the plane containing the center atom is 0.063 nm [13-15].

1.2.2 Polytypism of SiC

Silicon carbide crystal can be divided into multiple subunits called bases; each basis is constituted of atoms from one plan bounded to the other type of atoms on the next plane. Those two plans are denoted a bilayer. In a tetrahedral form, the basis is oriented around the center axis of the tetrahedron in two ways, by either a rotation to the left or a rotation to the right, as illustrated in Fig I.1 Thereby, we have three types of bases: bases rotated to the left denoted (A), bases rotated to the right denoted (C), and bases formed of one silicon atom and one carbon atom situated along the center axis denoted (B) [14-16].

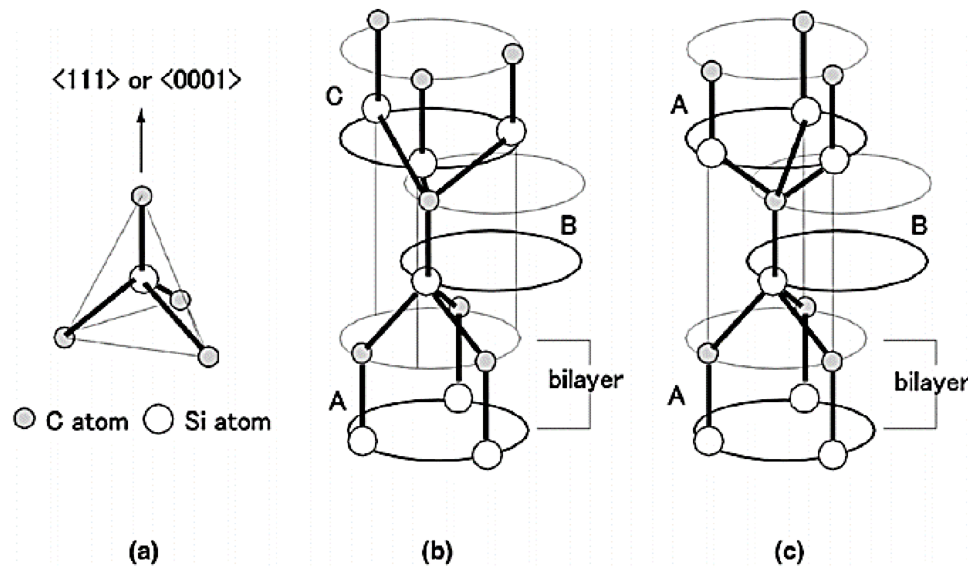


Figure 1.1 *illustration of the tetrahedral arrangement of silicon and carbon atoms in SiC crystals, pointing out the cubic sites (b), and the hexagonal sites (c) [16].*

The bases are stacked (on top of each other) along the center axis of the tetrahedron with two possible orientations of each basis, allowing for infinite possible arrangements. In fact, in each arrangement, we can identify the smallest repetitive pattern with a certain number of bases in it, by which we can entirely describe the structure, and each set of bases in the smallest repetitive pattern presents a certain number of symmetries. In this fashion, A SiC polytype is defined as a crystal system type associated with a certain repetitive pattern of bases. Indeed, more than 200 SiC polytypes are reported in the literature, with only three crystal systems for all polytypes, namely: hexagonal, cubic, and rhombohedral. Among all of those polytypes, the most common are three polytypes, expressly: 4H-SiC, 6H-SiC, 3C-SiC. The number at the beginning denotes the number of bases in the repetitive pattern, and the letter that comes after represents the crystal system of the polytype, H for hexagonal, C for cubic, R for rhombohedral [14-16].

Fig 1.2 shows the structures of 3C-SiC, 4H-SiC, and 6H-SiC, with bases symbolized as two black and white attached circles, the three types of basis are assigned each one a letter A, B, C. In this manner, we can distinguish that 3C-SiC pattern is ABC, and composed of three different successive bases. Whereas, the pattern of 4H-SiC structure is ABCB, and contains four bases. As for 6H-SiC pattern, it is constituted of six bases as follows: ABCACB. Certainly, the cubic crystal system of SiC is the simplest one, containing just one carbon atom and one silicon atom per unit cell, compared to (4C, 4Si) in 4H unit cell, and (6C, 6Si) in 6H unit cell.

All these crystallographic differences give rise to electrical, mechanical, thermal, and optical differences between SiC polytypes [14]. Table 1.1 summarizes some of these differences between the most common four polytypes at room temperature.

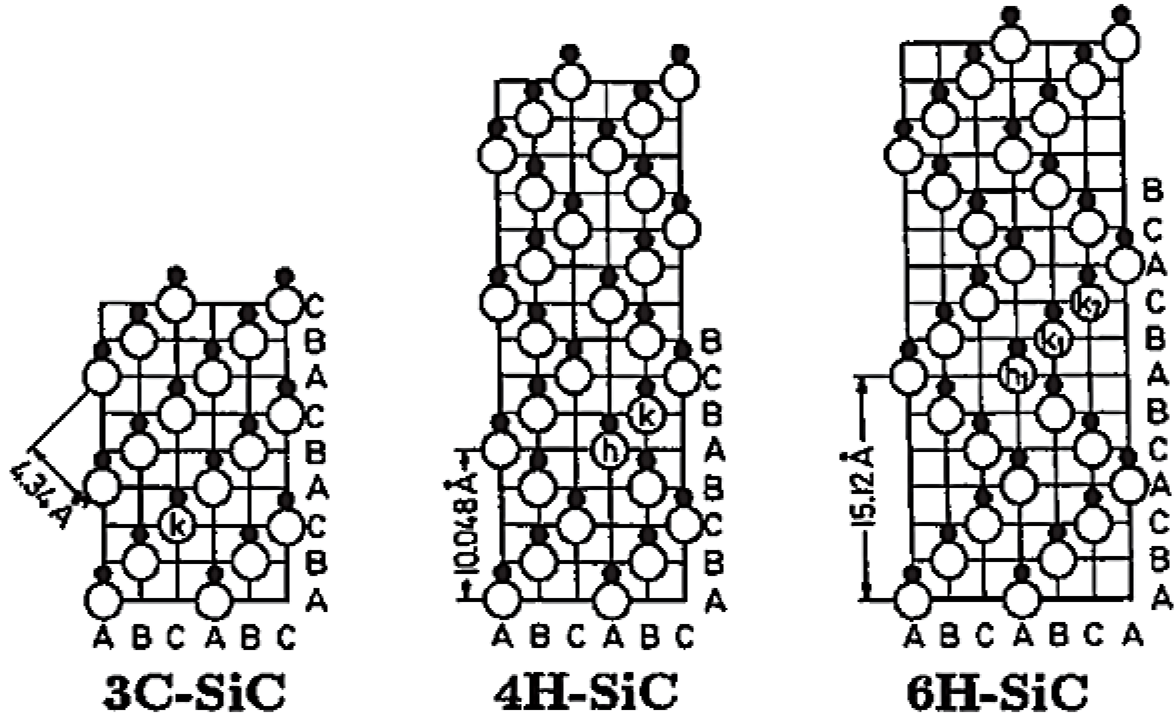


Figure 1.2. *Schematic of the main SiC polytype crystal arrangements [14].*

It can be seen from table 1.1 that 3C-SiC has one lattice constant, and that owing to its cubic unit cell, which is equally spaced in three dimensions. Since the unit cell of 4H and 6H polytypes is hexagonal, they have both two different lattice constants; one is the side of the basis of the hexagonal unit cell, and the other is the height of the hexagonal unit cell. It is also worth mentioning that differences in thermal conductivity between the mentioned polytypes are directly related to differences in the number of atoms per unit cell, which dictates pathways and number of phonons in the crystal. Moreover, the high indirect bandgap of SiC polytypes makes them less sensitive to ionizing radiations. Regarding the isotropy in the 3C polytype, it can be attributed to the fact that all the sites in the crystal are cubic (k), thus, all atoms of the crystal have the same surrounding environment. [14-18].

Table 1.1 *some basic physical and chemical characteristics of major SiC polytypes at room temperature* ***[16].***

Properties	4H-SiC	6H-SiC	3C-SiC
Lattice constant (nm)	0.307-1.005	0.308-1.512	0.43596
Bandgap (eV)	≈3.26	≈3.05	≈2.36
Density (g/cm^3)	3.21	3.21	3.213
Melting point (K)	3003	3003	2746
Thermal conductivity (W/cm.K)	3.7	4.9	3.63
Young's modulus (GPa)	220	220	250
Relative permittivity ε_r	10	9.7	9.6
Isotropy	No	No	Yes

1.2.3 Electronic properties of silicon carbide

The most relevant electronic features of semiconductors to the operating performance are mobility, critical electric field, and saturation velocity, as well as charge carriers lifetimes. Therefore, in this section, we will shed some light on those properties.

1.2.3.1 Mobility and drift velocity

One way of defining mobility is the amount of electric field required for charge carriers to reach a certain velocity inside the material. From the very beginning, we can see that mobility is a microscopic characteristic, which means that its value may changes at different points and in multiple directions. Hence, its accurate mathematical representation would generally be a matrix relating the charge carrier velocity to the applied electric field, but simplifications are usually achievable. While changes from one direction to another could be a mere characteristic of the material, the changes from one point to another is generally caused by local defects [19].

In that light, for hexagonal silicon carbide, mobility is anisotropic, which means it changes with respect to directions inside the crystal. Two main directions are widely explored in both experimental and theoretical aspects. I.e. the (0001) Si-face perpendicular to the c-axis, and the ($11\bar{2}0$) a-face parallel to the c-axis. At device scale, mobility is divided following regions, such as channel mobility, bulk mobility. For channel region, generally, the a-face ($11\bar{2}0$) exhibits higher

mobility than that of the Si-face (0001), when submitted to the same process conditions. In fact, mobility is dependent on temperature, doping concentration, and electric field. Moreover, SiC mobility is less dependent on temperature compared with silicon and GaN.

Regarding the three most common polytypes, 4H-SiC low electric field mobility is higher than that of 6H-SiC and 3C-SiC in doping concentration between $1*10^{16}$-$1*10^{18}$.

While, for high electric field, a nearly equal saturation velocity is observed with the three polytypes, barely over $2*10^{7}$ cm/s [19-21].

1.2.3.2 Critical electric field

The critical electric field is the maximum supported electric field at the breakdown. In addition, the blocking capability of any material has the bandgap as its key parameter, which is by definition the energy difference between the absolute minimum and maximum of the valence band and the conduction band, respectively, in the k-space. Several bandgap values are experimentally determined for silicon carbide depending on the investigated polytype. Results from optical absorption measurements show that the bandgap increases with increasing the ratio of hexagonal sites in the SiC polytype. For instance, 3C-SiC, which presents no hexagonal sites, has the lowest bandgap among all SiC polytypes with 2.2 eV. As for 6H-SiC, one quarter of the whole structure is in hexagonal sites with a bandgap of 3.02 eV. Next, we find 4H-SiC with half of its sites being hexagonal implying an elevated band gap of 3.26 eV. The wider bandgap is that of the polytype 2H-SiC showing only hexagonal sites, with a bandgap of 3.33 eV [14].

Actually, the wider the bandgap; the stronger is the critical electric field. For instance, the critical electric field of 4H-SiC is ten times higher than that of silicon having a bandgap of 1.1 eV. Generally, the critical electric field has a weak dependence on doping concentration, while it has a strong dependence on temperature. However, for silicon carbide the dependence on temperature is mitigated by an outstanding thermal conductivity [15].

1.2.3.3 Carrier lifetimes and impact ionization

The phenomenon of generation and recombination of charge carriers inside a semiconductor is an ongoing process in which an electron is promoted from the valence band to the conduction band living behind a hole; this pair of charge carriers has a lifetime before it is annihilated by recombination process to regain a state of equilibrium. The generation is due to many phenomena, such as thermal generation, photons, thermionic emission… etc. In addition, the leakage current in a reverse biased pn junction could be traced back to the generation recombination phenomenon,

where the generation lifetime determines the amount of the leakage current. Furthermore, generation lifetime can be employed to detect the existence of defects associated with short generation lifetimes, and having energies inside the bandgap. The significant point defects in silicon carbide, extensively discussed in the relevant literature are EH6/7 and Z1/2. Owing to its high band gap, silicon carbide has a very low intrinsic carrier generation at room temperature (low leakage current) of the order of 10^{-13} cm^{-3}, in contrast to 10^{15} cm^{-3} for silicon. The main generation recombination processes highlighted in the literature are Shockley-Read-Hall, and Auger. Whereas, average carrier lifetimes for SiC are between 1ns and 1µs [22].

Impact ionization is a generation process of free charge carries, enabled by high electric fields, such that generated charge carriers gain enough kinetic energy (at least $3/2*E_g$) to generate even more charge carriers by collisions in a way that is statistically significant. When the number of generated carriers is high enough, avalanche process could take place. Since the impact ionization process is by definition the inverse of Auger recombination where the mean free path is the counterpart of the impact ionization. Such path is traveled by accelerated electrons and holes with drift velocity V_n or V_p, respectively. The numbers of electrons and holes generated per charge carrier pair in that length are called impact ionization rates α_n, α_p, respectively [23]. The avalanche generation rate is given by:

$$G_{av} = \frac{1}{q} * (\alpha_n * J_n + \alpha_p * J_p)$$

From the famous Chynoweth formula, we have:

$$\alpha_{n,p} = a_{n,p} * e^{\frac{b_{n,p}}{E}}$$

Reported values of a_n, b_n and a_p, b_p for 4H and 6H polytypes are summarized in table 1.2

***Table 1.2** experimental impact ionization coefficients for 4H-SiC and 6H-SiC [23].*

	a_n	b_n	a_p	b_p
4H-SiC	$2.78*10^6$	$1.05*10^7$	$3.51*10^6$	$1.03*10^7$
6H-SiC	$1.66*10^6$	$1.27*10^7$	$5.18*10^6$	$1.4*10^7$

1.2.4 SiC/SiO$_2$ interface

Although, silicon carbide shows an outstanding multitude of physical properties, SiC-based MOS structures are far from matching those properties due to the poor SiC/SiO$_2$ interface. SiC,

among all compound semiconductors, is marked by an exclusive trait, which is a thermally grown native oxide layer with considerable dielectric capability. Two thermal oxidation processes have been used to grow an oxide layer on top of SiC wafers; one is known as dry O_2 oxidation, and the other is wet O_2 oxidation. Practically, the most commonly used is the dry O_2 oxidation. Unlike silicon, this oxidation results in a high trap density at the SiC/SiO_2 interface and near the interface, at least two orders of magnitude greater than that of silicon near the conduction band. Several types of defects are indicated in the literature, among others, carbon clusters at the interface, Si/C/O clusters, and silicon sub-oxides SiO_x, ($x < 2$). Mainly, they differ in physical nature, location, and energy levels. However, interface defects are of common existence with comparable distributions in the bandgap for different SiC polytypes [14, 24].

Several experiments have demonstrated an increase of interface traps density when the measurements are nearing the conduction band minimum. The most important traps with the more pronounced hindering effects are generally thought to be residual carbon clusters at the interface, near interface defects on the SiO_2 side, and the fluctuating nature of the SiC conduction band minimum at the interface proximity. In silicon, coulomb scattering is the mechanism proposed for charge mobility degradation related to electrically active defects. However, in SiC it is trapping of electrons that is responsible for carrier mobility degradation.

Regarding carbon residuals, the energy level whose spectrum is found to be correspondent to an sp^2 bounded carbon residuals is between 1.5-2 eV above the SiC valence band maximum. The carbon bounds are considered to be mid-products from the SiC oxidation process, with a density reaching in some cases $9*10^{11}$ $cm^{-2}.eV^{-1}$ forming what is called deep level impurity. If left untreated those C defects may contribute to the degradation of the channel mobility. As for defects due to conduction band minimum fluctuation, we have said earlier that stacking arrangement differences in silicon carbide polytypes are believed to be the root cause behind the bandgap diversity. Therefore, the multiple ways in which SiC surfaces could be attached to the SiO2 surfaces are regarded as an inherent cause for conduction band fluctuations at the interface. In fact, it is discovered that the conduction band minimum at the interface could fluctuate between 1.2 eV upwards and 0.3 eV downwards because of changes in the way in which the two surfaces are linked together at the same interface layer. Furthermore, those fluctuation points are viewed as scattering centers contributing to the low channel mobility in SiC-based MOSFETs [24-25].

The most hindering effect is shown with near interface defects. Although ambiguous, Attempts have been made to discover the origin of these defects, some authors have assigned them to carbon dimers and silicon interstitials which generate energy level similar to those observed with near interface defects. They are located on the SiO_2 side near the interface generating energy levels of about 2.77-2.8 eV below the SiO_2 conduction band edge with high density reaching $1*10^{13}$ $cm^{-2}.eV^{-1}$. These levels are certainly inside the conduction band of 6H-SiC. Whereas, In 4H-SiC these levels are below and above the conduction band minimum with a higher amount on the below side. Thus, the negative effect is more pronounced in 4H-SiC. In the silicon case, the interface traps mechanism of work is modeled by a simple thermal emission/capture process. However, in SiC the traps location near the interface implies that a tunneling process is involved. These traps are characterized by a shorter response time when close enough to the interface, that they affect carrier mobility, and a long response time when farther away, causing threshold instability [24-27].

In order for manufacturer to diminish the density of interfacial defects at SiC/SiO_2 interface, a recourse to post oxidation annealing by nitric oxide (NO), or nitrous oxide (NO_2) has to be made. When first discovered, this operation has revived interests in SiC-based devices after being traumatized by the interface low quality. This process has been shown to significantly lower the interface defects caused by thermal oxidation of silicon carbide.

Over the years, several recommendations have been established to reduce the interface defects density, such as; lowering oxidation temperature has always been linked to a decrease in interface defects density. Moreover, increasing the temperature of the post oxidation annealing in nitric oxide or nitrous oxide results in reduced interface defects. In addition, the deposition of a silicon layer on SiC wafers, and the oxidation of the silicon layer instead of the SiC surface to produce silicon dioxide with relatively lower temperatures is highly recommended to avoid carbon-related defects [13, 26].

1.3 Group III-nitrides

At present, the compound semiconductors called group III-nitrides are the second most important wide bandgap materials after silicon carbide. This family of materials shows a variety of attractive characteristics, which are at the basis of their importance, including the direct wide bandgap, the blue electroluminescence of GaN, as well as the high carrier mobility of InN, and the piezoelectric properties with the insulating capability of GaN and AlN. Unlike silicon and silicon carbide, the direct bandgap of this family made them suitable for optoelectronic applications.

These materials by means of bandgap engineering extends along a wide range of bandgap energy, namely from 1.9 to 6.2 eV covering the range from red to ultraviolet. Hence, providing a series of alloys, which have the necessary bandgap for blue/UV $LED_{s,}$ UV detectors, and laser diodes for data processing [28]. When both high frequency (GHz range) and high power output are required, group III-nitrides are the optimal recourse.

In fact, the molecular bounding is stronger, as the atomic weight is lower; which explains the strong atomic bounding of group III-nitrides constituted of a light N element. This strong bonding gives rise to robust mechanical and chemical properties. This family comprises GaN, AlN, and InN, as well as their alloys. The most important member of this family is GaN, from which alloys with Aluminum and Indium are issued to fabricate LEDs and diodes. Besides, GaN-based high electron mobility transistors ($HEMT_s$) are revolutionizing RF applications. Although thriving, GaN-based devices are far from reaching the corresponding theoretical limits. For instance, HEMTs have not meet one third of the theoretically assessed critical electric field ($3*10^6$ V/cm). This is essentially because of two roadblocks. The first one is the fact that mature GaN growth technology is only available as GaN-epilayers grown on either silicon, silicon carbide, or sapphire. Whereas the second is the device lateral structure and low dimensional quantum structure [29-30].

1.3.1 An overview on Group III-nitrides crystal structure

III-nitrides can crystalize in three different structures; zincblende, wurtzite, and salt rock (NaCl). The wurtzite (WZ) structure is constituted of two hexagonal-close-packed lattices displaced from each other along the c-axis by $\frac{3}{8}$ of the internal parameter u defined as the smallest distance between cations and anions along the c-direction. Furthermore, WZ is built around a hexagonal unit cell characterized by a height (c), and a squared basis of side (a).

Generally, the hexagonal III-nitrides have a stacking sequence of two repeating bases ABAB…etc. denoted 2H. While, the zincblende (ZC) structure of III-nitrides consists of cubic unit cells with a stacking sequence of three repeating bases ABCABC…etc. as shown by Figure 1.3. Moreover, WZ unit cell contains four atoms tetrahedrally bounded; of which two are nitrogen atoms, and the other two are III-metal atoms. On the other hand, ZC unit cell has two atoms, of which one is nitrogen atom, and the other is III-metal atom. Similar to group V semiconductors, atoms of III-nitrides crystals are, predominantly, linked to each other by covalent bounds, with an ionic component due to noticeable differences in electronegativity between III-metals and nitrogen. In addition, Wurtzite structure tend to be less covalent than zincblende structure. In general, WZ

structure is less symmetric than ZC structure, which means more parameters are required to describe the WZ structure. Conversely, WZ [0001] direction shows a striking similarity with ZC [111] direction. In fact, among all possible crystal structures of the III-nitrides, for ambient conditions, wurtzite structure has the lower total internal energy, as either bulk or epilayer. Therefore, it is thermodynamically stable. Regarding metastable zincblende structure of GaN and InN, it can be stabilized under convenient conditions as an epilayer grown on {011} faces of zincblende substrates such as silicon, silicon carbide, and gallium arsenide. However, III-nitrides crystalize in salt rock structure only when submitted to very high pressure. It is worth mentioning that most III-nitrides-based devices are fabricated using WZ crystals.

Zincblende and wurtzite structures of III-nitrides have, approximately, close bandgaps for the same material. For instance, The GaN wurtzite bandgap is 0.2 eV higher than that of GaN zincblende, and it corresponds to ultra violet spectrum (~360 nm), while znicblende bandgap corresponds to UV/violet spectrum (~383 nm). Unlike WZ structure, ZC bandgap can be easily cleaved [30-33]. Several specific planes in terms of polarity characterize both WZ and ZC structures. Among others, we can distinguish the polar planes of the WZ families: $\{0001\}$ and $\{1\bar{1}01\}$, with the ZC family $\{001\}$, along the c-direction, called c-planes. In addition, the non-polar planes of the WZ families: $\{11\bar{2}0\}$ called a-planes, and $\{1\bar{1}00\}$ called m-planes, with the ZC family $\{110\}$, perpendiculars to the c-plane. Finally, semi-polar planes which are identified by non-zero u, w, and z. components of the miller indices {u,v,w,z} of the wurtzite structure, like $\{11\,\bar{2}\bar{2}\}$ planes, $\{20\bar{2}1\}$ plans, and $\{10\bar{1}\bar{3}\}$ plans… etc. [34-35]. as illustrated in Figure 1.4.

The spontaneous polarization in III-nitrides is attributed to the absence of inversion centers. Table 13 summarizes the important physical parameters of both GaN and AlN.

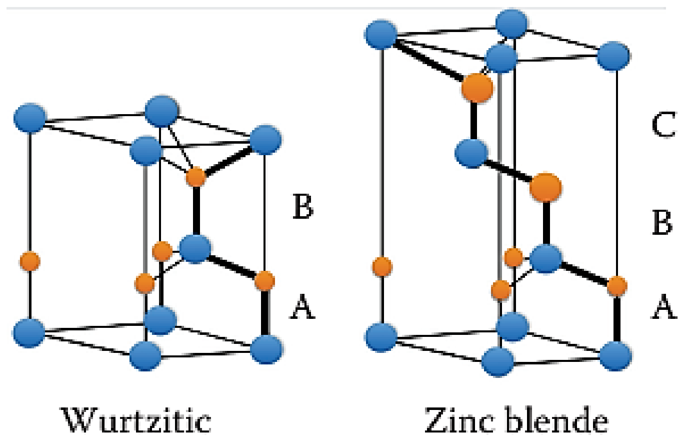


Figure 1.3 *Schematic of stacking sequences in both wurtzite and zincblende structures of III-nitrides [28].*

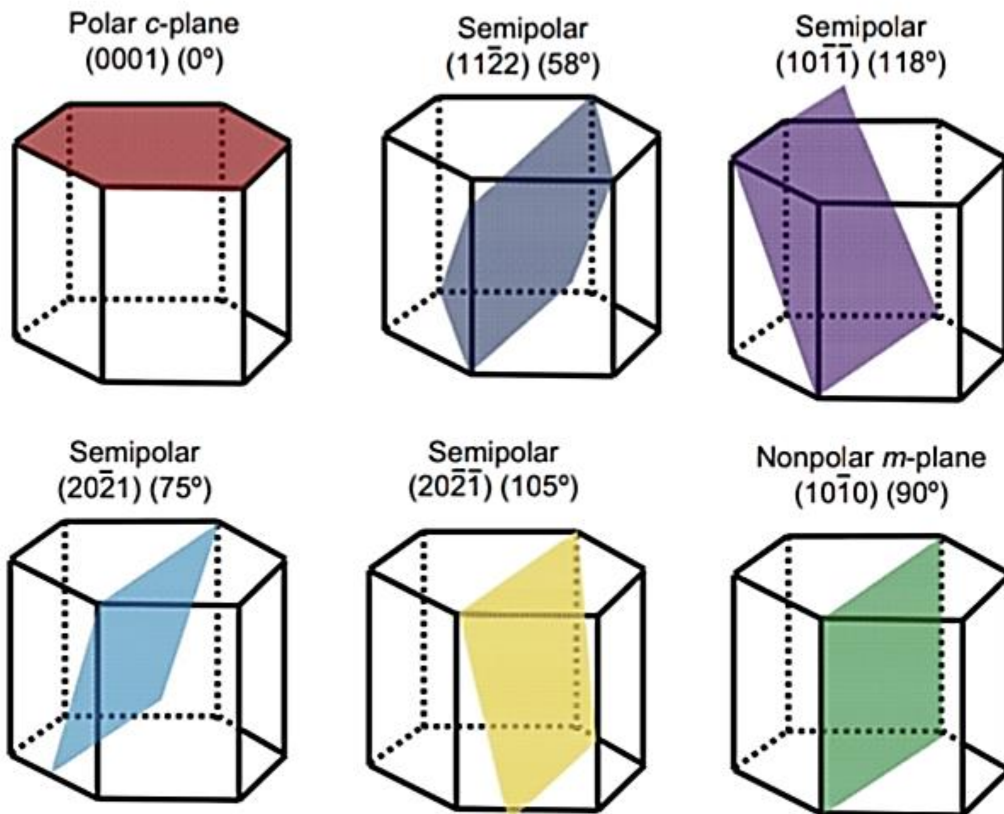


Figure 1.4 *Representation of some polar, non-polar, and semi-polar crystal planes with different inclinations in the wurtzite structure of the III-nitrides [34].*

Table 1.3 *Recapitulation of some physical properties of GaN, and AlN [28].*

	GaN	**AlN**
Molecular and atomic weight	83.73	40.99
Lattice constants (Å)	a=3.189 c=5.186	a=3.112 c=4.982
Bandgap (eV)	3.39 (bulk) 2.2 (epilayer)	6.2
Melting point (^{0}C)	1500	~2400
Thermal conductivity (W/cm.k) at 300 k	0.65	0.82
Density (g/cm^3)	6.15	3.23
Electron affinity (eV)	4.1	0.6

1.4 Gallium oxide

In the last years, we find gallium oxide (Ga_2O_3) among the newest wide bandgap materials; it was first introduced in 1952, and is still under research and development in the midst of a worldwide propensity towards developing materials with improved reliability for power applications. With an ultra-wide bandgap energy of 4.5-5.3 eV, gallium oxide is a representative of the next-level wide bandgap materials, having an expected critical electric filed greater than 7 MV/cm exceeding, by far, that of SiC and GaN. While the weakest point of gallium oxide properties is its low thermal conductivity of 0.23 W/K.cm. Surprisingly, the strongest property of gallium oxide with respect to SiC and GaN, from a technological standpoint, is the availability of a melt growth process to produce gallium oxide crystals with a melting point estimated at 1940 ^{0}C. Unlike gallium oxide, SiC and GaN are grown from vapor processes, adding more complication and cost [17, 36].

Various types of stable crystal polymorphs referred to as α-(corundum), β-(monoclinic), γ-(defective spinel), δ-(cubic), and ε-(hexagonal) characterize gallium oxide, of which the newest one is κ-Ga_2O_3. Among those polymorphs, β-Ga_2O_3 is substantially the more suited for electronic applications. This polymorph has attracted most of the research and development efforts regarding gallium oxide, and it is the most thermodynamically stable, and has a body-centered monoclinic

unit cell with a=1.223 nm, b=0.308 nm, and c= 0.58 nm. The angle between its c-axis and the basal plan is 104^0. It has two inequivalent sites for gallium atoms, specifically, one is a tetrahedral site, and the other is an octahedral site. The two gallium sites are denoted Ga(I) and Ga(II) in figure … in addition, the unit cell contains three different O-sites, with one as a tetrahedral coordination, and two as a trigonal coordination. These three O-sites are denoted in Figure 1.5 as O(I), O(II), O(III), respectively. The interionic distances between the unit cell different sites are as follows: 0.183 nm for Ga-O tetrahedral bound, 0.2 nm for Ga-O octahedral bound, 0.302 for O-O tetrahedral edge bound, and 0.284 nm for O-O octahedral edge bound [36-37]. Table I.4 summarizes some crystal properties of the other gallium oxide polymorphs.

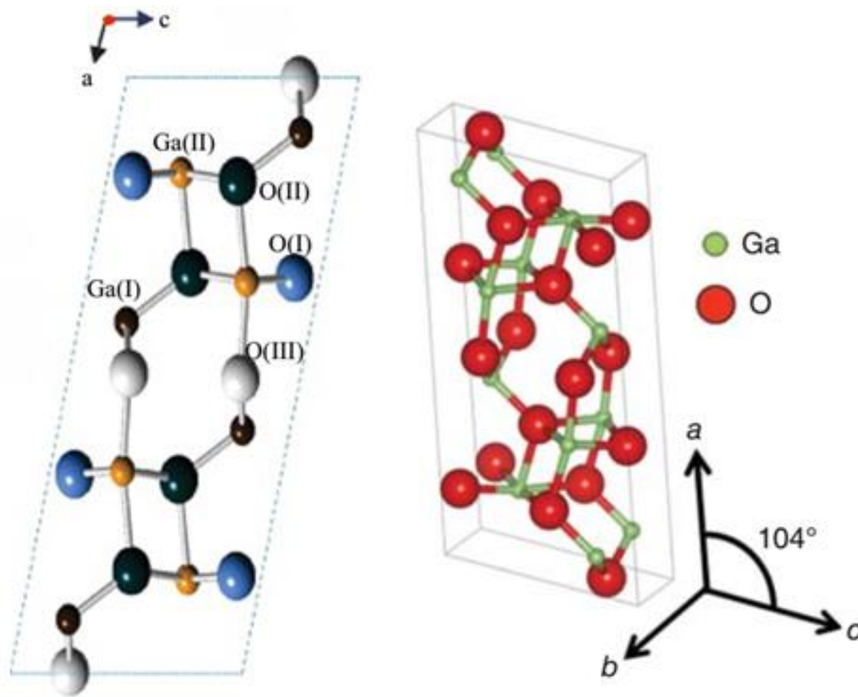


Figure 1.5 *Unit cell of β-gallium oxide showing gallium sites and O-sites following b-axis, with a 3D view following a-axis [17, 36]*

Table 1.4 A summary of some physical properties of gallium oxide polymorphs. [36]

Polytypes	Unit cell	Space group	Lattice constants (nm)	Bandgap (eV)
Α	Corundum	R-3c	a=0.49, c=1.34	5.3
Γ	Defective spinal	Fd-3/m	a=0.82	5.0
Δ	Cubic	Ia-3	a=1	-
Ε	Hexagonal	$P6_3mc$	a=0.29, c=0.92	5.0
Β	Monoclinic	C2/m	a=1.22, b=0.3, c=0.58	4.9

1.5 Power devices based on wide bandgap materials

From a technological point of view, wide band gap materials properties such as low intrinsic carrier concentration and high critical electric field are the basis of device properties like high temperature capability, low ON-resistance, and unipolar conduction up to several kilo-volts, implying lower conduction losses, lower switching losses, and higher switching frequency in comparison to silicon-based power devices. Those advantages could be translated into electronic systems with smaller cooler, smaller size, and less weight [38-41]. Figure 1.6 shows commercially

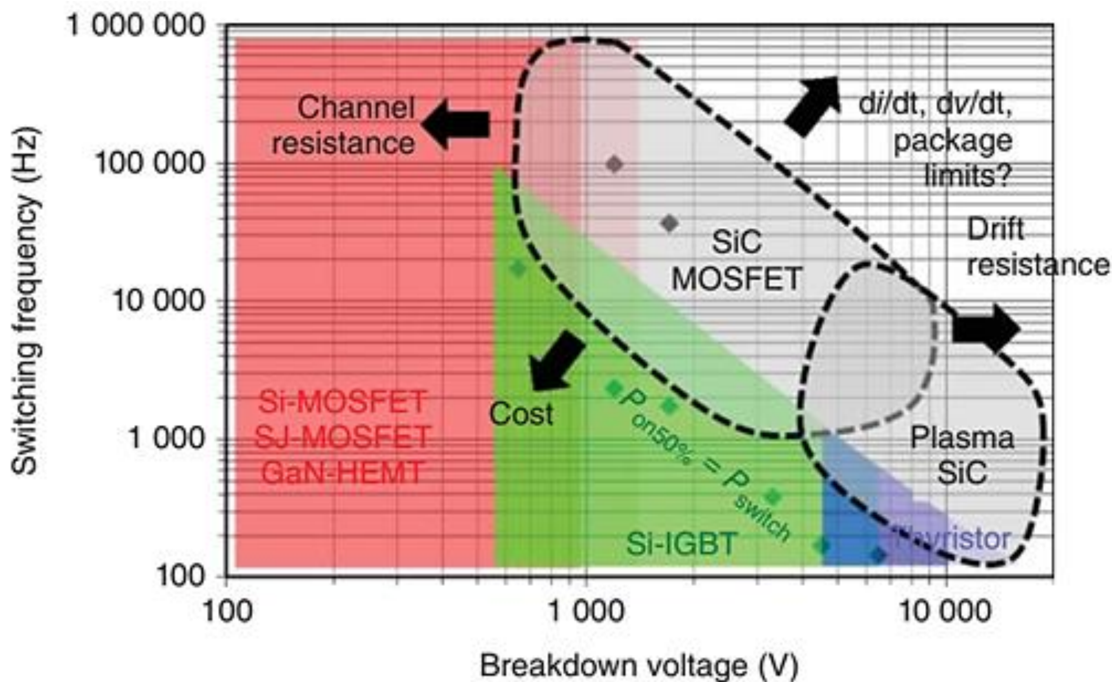


Figure 1.6 *Plot of reachable frequencies range for Silicon, SiC, and GaN devices versus their blocking capability. [17]*

available SiC-MOSFET and GaN-HEMT capabilities in terms of switching frequency and breakdown voltage with respect to commercially available silicon power devices.

1.5.1 Power MOSFET

Wide bandgap-based Power MOSFET is a unipolar device having the capability of carrying, exclusively, majority carrier current even when subject to voltages up to 6 kV, and high operating temperature of about 175 ^{0}C. This is achieved without the need for electron-hole-plasma to modulate the conduction and reduce the series resistance like the case of IGBTs, which burdens the device in terms of switching losses. Regarding the on-resistance in power MOSFETs, it changes with the different structures, for instance, the channel resistance accounts for more than half the on-resistance of a planar structure. Whereas, the drift resistance accounts for more than half the on-resistance of a trench structure. Moreover, power MOSFETs are characterized by high gate impedance consuming no current in the steady state, and does not allow second breakdown phenomenon like bipolar devices. When commutating from conducting to blocking states and vice versa, only majority carriers and capacitive carriers in power MOSFETs have to be removed, hence, the switching speed in such devices is devoid of any structural limitation in the device, unless limited by the circuit or the packaging. Nevertheless, power MOSFETs switching losses have the energy stored in the output capacitance during the off state as a minimum, which is inevitably lost when turning into the on state. With such performances, power MOSFETs are capable to reach switching frequencies of several hundreds of kilohertz.

In this context, power MOSFETs are considered as one of the most helpful devices for power electronic applications such as switched-mode power converters, industrial drives, smart grids, traction, inductive heating, photovoltaic …etc. Owing to low on-resistance, high breakdown characteristics, and fast commutation. For this reason, power MOSFET has been the subject of intensified research, where various strategies such as electric field modulation layers (L-shaped p-layers, float islands, and shielded regions), trench gate, and super junction were proposed to achieve further improvements concerning the device electrical and breakdown characteristics [42-46]. III-V materials and Diamond were used to design power transistor devices, demonstrating the highest performances but the elaboration cost is still high and new strategies are required [47-49]. Following this direction, researches are focusing on exploring alternative wide band-gap critical raw materials-free (CRM-free) for reducing the fabrication cost of power MOSFET devices [49-51]. As a potential candidate, silicon carbide (SiC) CRM-free nontoxic material has been

extensively used for the design of power MOSFET devices, showing favorable electrical, breakdown and thermal reliability performances [44-49], [49-52].

Much research interest has been paid to improving the SiC power MOSFET performance through proposing new design methodologies. Despite this, SiC power MOSFET still require further improvements regarding the device electrical and switching performances. Furthermore, the use of complicated structure with several abrupt junctions can increase the fabrication cost of these devices. In addition, applications requiring high operating temperature are still hindered by packaging materials, even more as far as silicon carbide is concerned. Therefore, new design strategies should be considered for the development of efficient, low-cost SiC power MOSFETs.

While searching for novel strategies for suppressing the high thermal budget, we came across an interesting technology based on Junctionless (JL) aspect. The latter suggests getting rid of junctions by considering a uniformly doped channel in several MOSFET structures, where interesting characteristics are achieved.

1.5.2 Insulated gate bipolar transistor (IGBT)

Silicon power MOSFET in the 70s was a high-performance device when the targeted voltage is 200 V and lower, because in this range, the series on-resistance remains limited, and conduction losses are still affordable. However, for higher voltages the drift region has to be significantly increased, resulting in elevated on-resistance, and accentuated parasitic phenomena like parasitic capacitances, reducing power-handling capability, in addition to large chip size. Those compromised performances of silicon power MOSFET beyond 200 V motivated the scientific community to propose solutions, and the most prominent at that time was to add a minority-carrier injecting junction in the drift region to the drain edge, decreasing, as such, the on-resistance by these additional charge carriers. Those changes gave birth to what was called insulated gate bipolar transistor (IGBT), which is viewed as a combination between a power MOSFET and a bipolar transistor, such that it is controlled by a power MOSFET structure and the conductivity of the MOSFET drift region is modulated by an inherent pnp bipolar transistor. The IGBT structure was an improvement of the silicon power MOSFET such that it can support higher voltages with reduced on-resistance at the cost of a lower switching capability, and higher switching losses, due to the necessity to remove the minority carriers in the drift region for every switching cycle. For instance, 1.2 kV IGBT is limited to a frequency of 20 kHz. However, IGBT can be optimized following its application requirements, as for low frequency conditions high electron-hole-plasma

concentration is preferable to reduce conduction losses, and when high frequency is prerequisite, low electron-hole-plasma should be adopted to the extent in which conduction losses are affordable [17, 53]. In fact, the IGBT low conduction losses with respect to power MOSFET hold true only in case of high current level where power MOSFET suffers from high forward voltage drop. Conversely, power MOSFET can conduct current in both directions owing to the body diode, whereas IGBT can conduct current only in one direction due to the additional pn junction on the drain side. Furthermore, IGBT structure is hindered by a higher delay time in comparison to power MOSFETs, which is translated into voltage overshoots during turn-on time, and tail current during turn-off time. Although dominant in power devices market due to its low cost, silicon IGBT is undergoing a replacement by silicon carbide MOSFETs, which have the ability to reach comparable blocking ratings without compromising switching performances. For instance, 1.2 kV SiC-MOSFET can have a commutation frequency of 1MHz. Nevertheless, the logic behind the use of the IGBT structure in the silicon case is still applicable to the silicon carbide power MOSFET case for voltages higher than 20 kV, where the same problems with the silicon power MOSFET for voltages higher than 200 V rise again. Thereby, SiC-IGBT technology is expected to be on a commercial level in the near future [17, 54].

1.5.3 High electron mobility transistor (HEMT)

High electron mobility transistor is a lateral transistor controlled by a gate, and has on one side a drain electrode, and on the other side a source electrode. This transistor is realized only by means of compound semiconductors such as AlGaAs/GaAs, AlGaN/GaN. It was first introduced in the 70s based on AlGaAs/GaAs for RF applications by means of molecular beam epitaxy (MBE) [55]. In the early 90s, HEMTs was developed based on nitrogen instead of arsenic, by virtue of metalorganic chemical vapor deposition (MOCVD), with demonstrated operating frequencies of 11 GHz and 35 GHz [36, 55]. The conduction mechanism of HEMTs is not based on a channel created by an inversion bias in doped regions like MOSFETs, but rather it is based on a channel created with no intentional doping in a heterojunction, that is a junction between two different materials, namely AlGaN/GaN. In this type of heterojunctions, the difference in bandgap energy fosters the creation of a quantum well at the interface between the two materials.

In addition, the presence of both a piezoelectric polarization in AlGaN due to the lattice mismatch with GaN, and a spontaneous polarization, cause charge carries to exist at the interface countering the effect of those polarizations, such that electrons are confined into this quantum well inciting

the emergence of the so-called two dimensional electron gas (2DEG) [17, 36, 55-56]. In such case, the absence of doping impurities along with the 2D motion of the free carriers contribute to the mean free path increasing, which results in very high mobility around 2000 $cm^2/V.s$, hence the name high electron mobility transistor. Moreover, the mobility could be controlled by adjusting the thickness of the AlGaN layer and the amount of aluminum in it.

As for the current, it flows along the source-drain direction few nanometers away from the surface of the device, typically 20 nm-50 nm depending on the thickness of the AlGaN layer. Inherently, the most basic HEMT is a normally-on structure (depletion mode structure). In terms of safety together with easiness of control, normally-off structures are preferred. From a switching standpoint, capacitances in the HEMT structure are significantly lower in comparison to those of silicon devices for the same ratings. Giving the fact that all commercially available AlGaN/GaN HEMTs are lateral devices, the blocking capability can only be increased by means of extension of the drain-to-source length or by increasing the thickness of the buffer layer. In that context, GaN HEMTs are thriving for applications in the range of 650 V and below, where they are implemented in inverters for photovoltaic, amplifiers, and low voltage power supplies with outstanding lower size… etc. [56-57].

1.6 Power converters based on wide bandgap devices

The use of wide bandgap materials in switches of power converters is mediated through the need for reducing the size of the passive elements (inductances, capacitances, transformers) by going up in frequency, and rising the operating power, reaching, as such, high power density. Furthermore, the adoption of wide bandgap-based devices decreases power losses when elevating the switching frequency is required, and makes high operating temperatures easier to deal with [58-60].

1.6.1 Inverters

An inverter is a power converter, which transforms the power from direct to alternating with imposed output voltage or current, of which the frequency and the magnitude could be fixed or variable. Inverters are considered with respect to the input type as current source inverters (CSI), and voltage source inverters (VSI). They are generally controlled by pulsed width modulation (PWM) technique. Practically, inverters are building blocks of modern industry, as we find them in ac motor drives, photovoltaics, traction, induction heating, power supplies … etc.

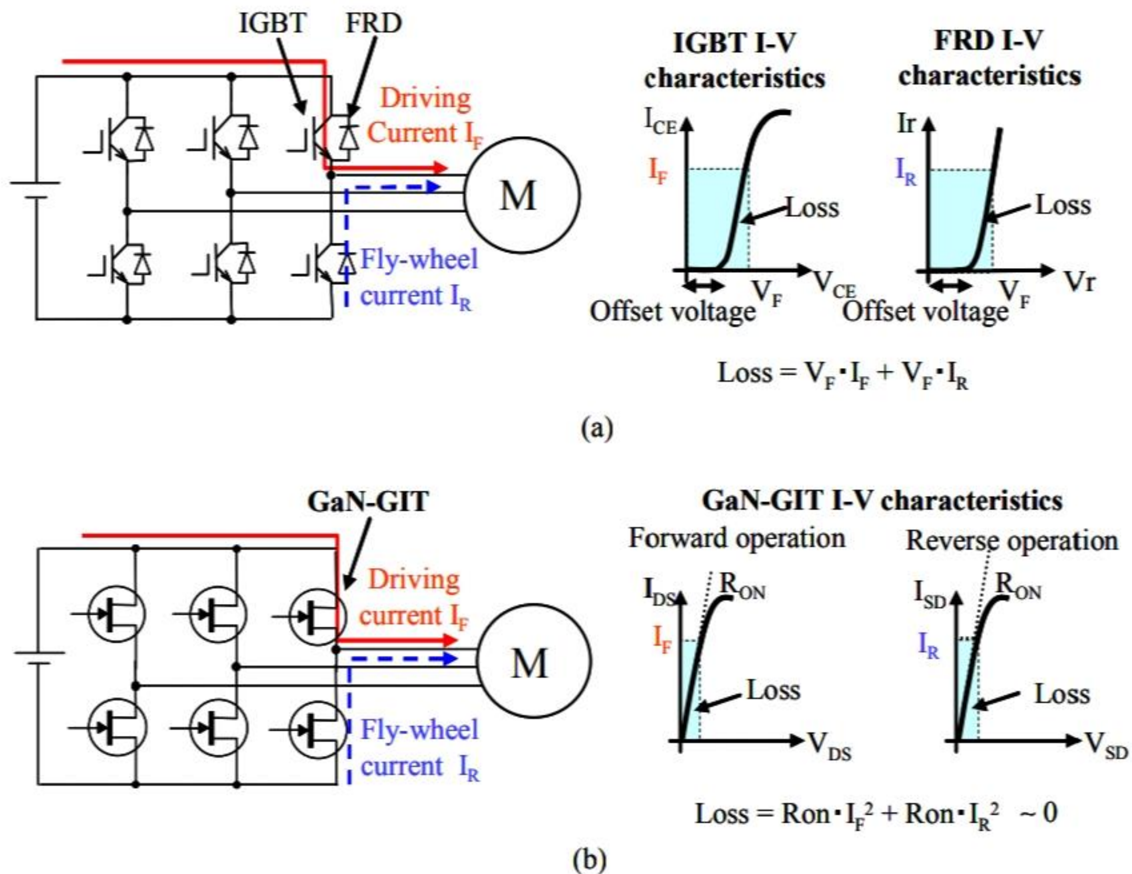


Figure 1.7 *Functioning and power losses of (a) an inverter based on IGBTs and (b) an inverter based on normally off GaN transistors called gate injection transistors (GITs). [61]*

Figure 1.7 shows (a) an inverter based on IGBTs and (b) an inverter based on normally off GaN transistors called gate injection transistors (GITs). Initially, the employment of GaN-based transistors in the inverter dispose the circuitry from the necessary flywheel diodes in the IGBT case, because GITs are bidirectional devices, which is translated into less conduction losses, more available space, and reduced cost. Moreover, offset voltage is a characteristic of IGBTs, which results in increased conduction losses. Conversely, GITs have no offset in drain voltage, which allows them to operate with lower losses. Generally, GaN-based transistors have lower series resistance owing to the heterojunction, surpassing the effect of Si-IGBTs modulating layer. At low power, around 1kW this GaN-based inverter proves an efficiency of 99.3 % compared to 98.5 % in the IGBT inverter, and reduced total losses of about 60 % with 6.8 W compared to 14.5 W in the IGBT inverter [17, 36, 61].

1.6.2 Choppers

Choppers are power converters, which act on a DC input power and deliver a DC output power with different current and voltage values from the input. The simplest forms of DC-DC converters are boost converters, which elevate the voltage or the current in output, and buck converters reducing the voltage or the current in output. These step up and step down of the output voltage and current are carried out by virtue of an inductance. A combination of the two type is called a buck-boost converter and delivers either an amplification or an attenuation of the input.

Figure 1.8 is a schematic of a boost converter based on silicon carbide MOSFET applied to PV panels. The 1.2 kV SiC-MOSFET was compared to a high-performance 900 V silicon super-junction MOSFET called CoolMOS in a boost converter. The SiC MOSFET outperformed the CoolMOS in terms of total power losses with ~ 25 W at 250 kHz compared to ~ 43 W at 250 kHz, and the SiC MOSFET has shown a lower junction temperature around 78 ^{0}C at 250 kHz, whereas the CoolMOS junction temperature has increased drastically to 200 ^{0}C at 250 kHz. The SiC

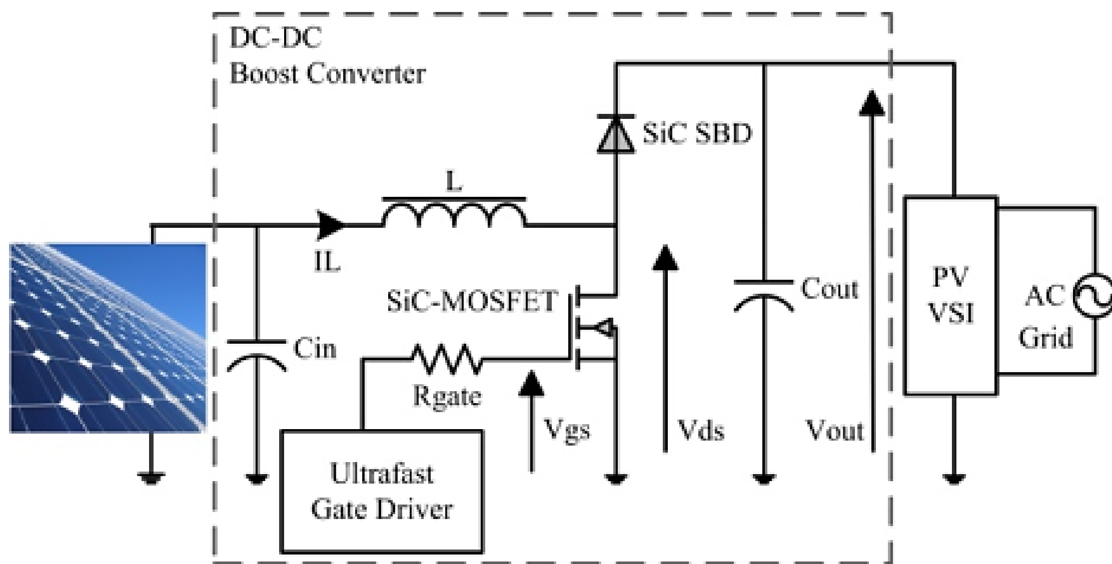


Figure 1.8 *Photovoltaic panel related to DC-DC boost converter based on SiC-MOSFET [62].*

MOSFET efficiency of 95.5% was independent of the frequency between 100-250 kHz. Compared to frequency dependent efficiency of the CoolMOS with 95 % at 100 kHz and 92.5% at 250 kHz due to the rise of power losses [62]. Besides, a flyback (buck-boost) converter based on SiC-MOSFET switches is reported as successful in [63] with 10 MHz switching frequency.

1.6.3 Rectifiers

A rectifier is a converter, which transforms an alternating source of power into a direct source of power; there are controllable rectifiers based on thyristors, IGBTs, and MOSFETs, as well as uncontrollable rectifiers based on diodes. The basic types of rectifiers are half wave rectifiers, and full wave rectifiers.

Figure 1.9 (a) represents a bridgeless PFC (power factor correction) converter called totem-pole converter based on (1.2 kV/36 A) SiC MOSFETs, controlled by means of PWM signals. The SiC MOSFET switches in this converter deliver a 3.3 kW of power. Moreover, this converter has a voltage conversion capability to transform a single phase alternating 86-256 V source into a regulated direct 300-600 V source at a switching frequency of 100 kHz. This converter performs a power conversion between an electric vehicle and the grid. In addition, the converter is capable to operate safely in continuous current mode (CCM) owing to the low reverse recovery charge of the SiC-MOSFET. The experimental efficiency of this converter peaks up at 1kW to reach 99.2 % and decrease to 98.8 % at 2 kW for 220 V alternating voltage source [64].

Figure 1.9 (b) is a forecast of the previous converter type with a combination of GaN-based transistors and SiC-MOSFETs. It is estimated that this expected converter would reach a power independent efficiency of 99.3 % with higher switching capability [59].

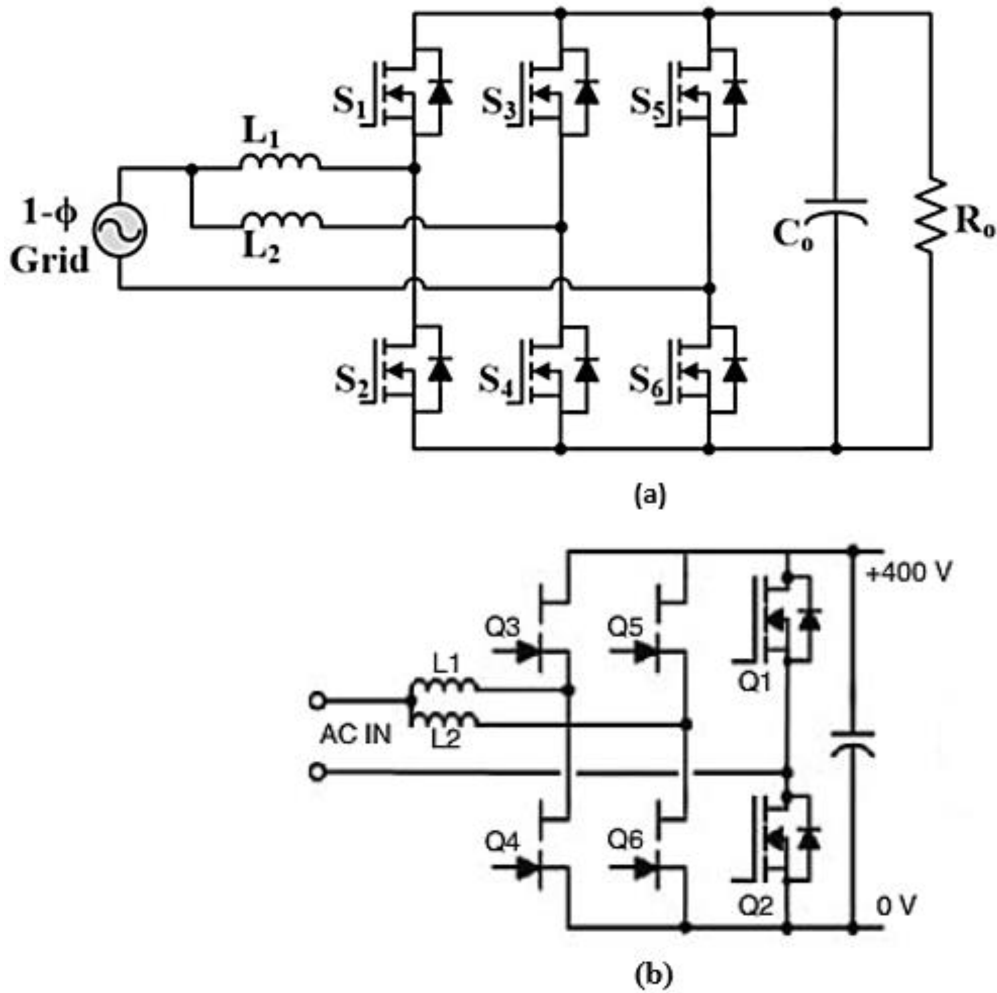


Figure 1.9 *A schematic of (a) Bridgeless totem-pole interleaved power factor correction converter intended for CCM functioning and based on SiC-MOSFETs, (b) Bridgeless totem-pole PFC converter intended for TCM functioning and based on GaN-transistors and SiC-MOSFETs. [59, 64]*

1.7 Conclusion

In this chapter, we have presented two sets of materials, the SiC family, and the III-nitrides family, together with gallium oxide. The SiC electrical and crystal properties provide a basis for the employment of SiC in the remainder of this thesis, and a justification for the choice of this material. Furthermore, the demonstration of III-nitrides properties serves as a good counterpart for comparison with the most important competitor in both the scientific research and in the industry. As for gallium oxide, it represents one of the newest introduced wide bandgap materials. In this light, silicon carbide properties and growth technology maturity allow him to be the silicon successor in the power range. However, the only limitation to the wide spread adoption of silicon carbide in power devices is the high cost of its fabrication compared to silicon. Regarding III-nitrides, they are well established in the industry as epilayer materials, used as first choice whenever power is requested with high frequency (Mega Hertz-Giga Hertz). However, the full potential of these materials cannot be achieved until a mature cost-effective technology of their native bulk growth is available. Following the same logic, a section on wide bandgap-based devices and power converters is presented, with a brief overview on SiC-MOSFET as it is the core subject of our contribution, and GaN HEMTs with silicon IGBTs as SiC-MOSFET rivals in both the scientific research and the market of power converters like inverters, choppers, and rectifiers. In that market, wide bandgap-based devices have been demonstrated to be both the most efficient at present and promising in the future.

1.8 References

[1] Kazuhiro Mochizuki. Vertical GaN and SiC Power Devices. Artech House, 2018.

[2] L. B. Drissi, F. Z. Ramadan, H. Ferhati, F. Djeffal and N. B.-J. Kanga, New highly efficient 2D SiC UV-absorbing material with plasmonic light trapping, Journal of Physics Condensed Matter vol. 32, pp. 025701, 2020.

[3] Kadri, A., Ferhati, H., & Djeffal, F. Giant responsivity of a new optically controlled graphene UV-phototransistor using graded band-gap ZnMgO gate. Sensors and Actuators A: Physical, 325, 112701, 2021.

[4] Ferhati, H., & Djeffal, F. Giant responsivity of a new InGaZnO ultraviolet thin-film phototransistor based on combined dual gate engineering and surface decorated Ag nanoparticles aspects. Sensors and Actuators A: Physical, 318, 112523, 2021.

[5] H Ferhati, F Djeffal, A. Benhaya, N. Martin, Highly sensitive, ultra-low dark current, self-powered solar-blind ultraviolet photodetector based on ZnO thin-film with an engineered rear metallic layer, Materials Science in Semiconductor Processing, vol. 110, 104957, 2020.

[6] Gourab Majumdar, Ikunori Takata. Power Devices for Efficient Energy Conversion. Pan Stanford Publishing, 2018.

[7] Francesco Iannuzzo. Modern Power Electronic Devices: Physics, Application and reliability. IET press, 2020.

[8] Muhammad H.Rashid. Power Electronics: Devices, Circuits and Application. Pearson Press, 2014.

[9] Alberto castellazzi, Andrea Irace. SiC Power Module Design: Performance, Robustance and reliability. IET press, 2022.

[10] Xiaoqing Song, Alex Q. Huang, Meng-Chia Lee, Chang Peng. *High Voltage Si/SiC Hybrid Switch: An Ideal Next Step for SiC*. IEEE Proceedings of the 27th International Symposium on Power Semiconductor Devices & IC's, Kowloon Shangri-La, Hong Kong, pp. 289-292, 2015.

[11] Vipindas Pala, et al. 10 kV and 15 kV Silicon Carbide Power MOSFETs for Next-Generation Energy Conversion and Transmission Systems. IEEE, Energy Conversion Congress and Exposition (ECCE), Pitsburg, USA, pp. 449-454, 2014.

[12] Arendt Wintrich, Ulrich Nicolai, et al. Application Manual: Power Semiconductors. ISLE Verlag press, 2015.

[13] Zhe Chuan Feng. Handbook of silicon carbide materials and devices. CRC press, 2023.

[14] Jiyang Fan, Paul k chau. Silicon carbide nanostructures: fabrication, structure, and properties. Springer press, 2014.

[15] Laurence Latau-Romain, Maelig Ollivier. Silicon Carbide one-dimensional nanostructures. ISTE Ltd and John Wiley & Sons, 2015.

[16] Kiyoshi Takahashi, Akihiko Yoshikawa, Adarsh Sandhu. Wide bandgap semiconductors: Fundamental Properties and Modern Photonic and Electronic Devices. Springer press, 2007.

[17] Peter Wellmann, Noboru Ohtani, Roland Rupp. Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications. Wiley press, 2022.

[18] Peter J. Wellmann. Power Electronic Semiconductor Materials for Automotive and Energy Saving Applications – SiC, GaN, Ga2O3, and Diamond. Journal of Inorganic and General Chemistry, 643, 1312–1322, 2017.

[19] Gang Liu, et al. Enhanced Inversion Mobility on 4H-SiC (1120) Using Phosphorus and Nitrogen Interface Passivation. IEEE Electron Device Letters, vol. 34, pp. 181-183. 2013.

[20] Maria Cabello, et al. Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review. Materials Science in Semiconductor Processing, vol. 78, pp. 22-31, 2018.

[21] Saeed Anwar, et al. Characterization and Comparison of Trench and Planar Silicon Carbide (SiC) MOSFET at Different Temperatures. IEEE Transportation Electrification Conference and Expo (ITEC), Long Beach, USA, pp. 1039-1045, 2018.

[22] Matthew J. Marinella, et al. Carrier Generation Lifetimes in 4H-SiC MOS Capacitors, IEEE Transactions on Electron Devices, vol. 57, pp. 1910-1923, 2010.

[23] W. S. Loh, et al. Impact Ionization Coefficients in 4H-SiC. IEEE Transactions on Electron Devices, vol. 55, pp. 1984-1990, 2008.

[24] Hamid Amini Moghadam, et al. Active defects in MOS devices on 4H-SiC: A critical review. Microelectronics Reliability, vol. 60, pp 1-9, 2016.

[25] Peyush Pande, et al. Electrical characterization of SiC MOS capacitors: A critical review. Microelectronics Reliability, vol. 112, 2020.

[26] Yifan Jia, et al. Infuence of various NO annealing conditions on N‑type and P‑type 4H‑SiC MOS capacitors. Journal of Materials Science: Materials in Electronics. vol. 30, 10302–10310, 2019.

[27] B.C. Johnson, et al. Optically Active Defects at the SiC/SiO2 Interface. Physical Review Applied, vol. 12, iss. 4, 2019.

[28] Fabrizio Roccaforte, Mike Leszczynski. Nitride Semiconductor Technology. Wiley-VCH press, 2020.

[29] Matteo Meneghini, et al. Power GaN Devices: Materials, Application and Reliability. Springer press, 2017.

[30] Farid Medjdoub, et al. Gallium Nitride (GaN): Physics, Devices, and Technology. CRC press, 2016.

[31] Wengang (Wayne) Bi. Handbook of GaN Semiconductor Materials and Devices. CRC press, 2018.

[32] Hadis Markoç, Handbook of Nitride Semiconductors and Devices. Wiley-Vch press. 2008.

[33] R. Szweda. Gallium nitride and related wide bandgap materials and devices: a market and technology overview 1998-2003. Elsevier press, 2000.

[34] Morteza Monavarian, et al. A Decade of Nonpolar and Semipolar III-Nitrides: A Review of Successes and Challenges. Physica Status Solidi, vol. 216, issue. 1/1800628. 2018

[35] Pierre Ruterana, et al. Nitride Semiconductors: Handbook on Materials and Devices. Wiley-Vch press. 2003.

[36] Fan Ren, Stephen J Pearton. Wide bandgap semiconductor-based electronics, IOP publishing, 2020.

[37] Stephen Pearton, Fan Ren, Michael Mastro. Gallium oxide: Technology, Devices and Applications. Metal oxides series, Elsevier press, 2018.

[38] Fan Ren, John C. Zolper. Wide energy bandgap electronic devices. World Scientific, 2003.

[39] H. Ferhati and F. Djeffal, Enhanced performance of ultraviolet photodetector based on sputtered ZnO/Au/ZnO multilayer structure, Superlattices and Microstructures 134, 106225, 2019.

[40] Ferhati, H., Djeffal, F., & Drissi, L. B. Enhanced infrared photoresponse of a new InGaZnO TFT based on Ge capping layer and high-k dielectric material. Superlattices and Microstructures, 156, 106967, 2021.

[41] H Ferhati, F Djeffal, Enhanced optical and electrical performances of UV-phototransistor using graded band-gap ZnMgO photosensitive gate, Journal of Computational Electronics, 17 (3), 1181-119, 2018.

[42] Hongyu Yu, Tianli Duan. Gallium Nitride Power Devices. Pan Stanford Publishing, 2017.

[43] Rakesh Vaid et al. A novel trench gate floating islands power MOSFET (TG-FLIMOSFET): Two-dimensional simulation study. Microelectronic Engineering, 88, 11, pp. 3316–3326, 2011.

[44] M. Kong, et al. A novel SiC high-k superjunction power MOSFET integrated Schottky barrier diode with improved forward and reverse performance. J. Semicond., vol. 44, pp. 052801, 2023.

[45] Y. Hu, et al. Numerical investigation on L-shaped vertical field plate in high-voltage LDMOS. Results Phys., vol. 15, pp. 102547, 2019.

[46] H. Ferhati, F. Djeffal. High-Responsivity MSM Solar-Blind UV Photodetector Based on Annealed ITO/Ag/ITO Structure Using RF Sputtering. IEEE Sens. J., vol. 19, pp. 7942 - 7949, 2019.

[47] S.-H. Yi, et al. High Performance Metal-Gate/High-k GaN MOSFET with Good Reliability for Both Logic and Power Applications. IEEE J. Electron Devices Soc., vol. 4, pp. 246-252, 2016.

[48] J. Sahoo, R. Mahapatra. Effect of Dummy Gate Bias on Breakdown Voltage and Gate Charge of a Novel In0.53 Ga0.47 As/InP Trench-Gate Pentode Power Device. IEEE Trans. Device Mater. Reliab., vol. 23, pp. 269-275, 2023.

[49] J. Tsunoda, et al. 580 V Breakdown Voltage in Vertical Diamond Trench MOSFETs With a P− -Drift Layer. IEEE Electron Device Lett., vol. 43, pp. 88-91, 2022.

[50] C. Langpoklakpam, et al., Review of Silicon Carbide Processing for Power MOSFET. Crystals, vol. 12, pp. 245, 2022.

[51] B. Zerroumda, F. Djeffal, S. Benaggoune, H. Ferhati. Performance assessment of a novel 4H–SiC junctionless planar power MOSFET towards improving electrical properties. Micro and Nanostructures, vol. 169, pp. 207346, 2022.

[52] B Zerroumda, H Ferhati, F Djeffal, S Benaggoune. A novel high-performance junctionless 4H-SiC trench MOSFET with improved switching characteristics. Microelectronic Engineering, vol. 277, pp. 112011, 2023.

[53] N. Iwamuro, T. Laska. IGBT History, State-of-the-Art, Future Prospects. IEEE Transactions on Electron Devices, vol. 64, pp. 741-752, 2017.

[54] N. Iwamuro. Recent Progress of SiC-MOSFETs and Their Futures-Competion with state-of-the-art Si-IGBT. International Conference on Electronics Packaging (ICEP), pp. 260-264, 2019.

[55] Stephen J. Pearton. Wide bandgap semiconductors: Growth, Processing and Applications. William andrew publishing, 2000.

[56] Gerrit Lükens. Normally-off Transistor Topologies in Gallium Nitride Technology. Phd Dissertation, RWTH Aachen University, 2020.

[57] E. A. Jones, F. F. Wang, D. Costinett. Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges. IEEE Journal of Emerging and Selected Topics in Power Electronics. vol. 4, pp. 707-719, 2016.

[58] G. Jia Su. Comparison of Si, SiC, and GaN Based Isolation Converters for Onboard Charger Applications. IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1233-1239, 2018.

[59] G. Deboy, et al. Si, SiC, and GaN Power Devivces: an Unbiased View on Key Performance Indicator. IEEE International Electron Devices Meeting (IEDM). pp. 20.2.1-20.2.4, 2016.

[60] A. Choudhury. Present Status of SiC Based Power Converters and Gate Drivers- A Review. International Power Electronics Conference (IPEC). pp. 3401-3405, 2018.

[61] Morita, T. et al. 99.3% Efciency of Three-Phase Inverter Using GaN-Based Gate Injection Transistors. IEEE Applied Power Electronics Conference and Exposition (APEC), p. 481, 2011.

[62] Omid Mostaghimi, Design and Performance Evaluation of SiC Based DC-DC Converters for PV Applications. IEEE Energy Conversion Congress and Exposition (ECCE). pp. 3956-3963, 2012.

[63] K. Hashimoto, et al. A Flyback Converter with SiC Power MOSFET Operating at 10 MHz: Reducing Leakage Inductance for Improvement of Switching Behaviors. International Power Electronics Conference (IPEC). pp. 3757-3761, 2018.

[64] Y. Tang, et al. A Bridgeless Totem-pole Interleaved PFC Converter for Plug-in Electric Vehicles. IEEE Applied Power Electronics Conference and Exposition (APEC). pp. 440-445, 2016.

Chapter 2

Performance assessment of a novel 4H-SiC Junctionless planar power MOSFET towards improving electrical properties

Abstract- *In this chapter, a novel 4H-SiC power MOSFET structure based on junctionless (JL)concept is proposed. The proposed device is investigated using accurate numerical models based on Atlas TCAD device simulator. It is revealed that the use of cost-effective junctionless structure can allow overcoming problems related to power MOSFET channel resistance, which results in a high figure of merit (FoM) ($BV^2/R_{on,sp}$= 2676/5.78= 1236) without the need of lowering the drift region resistance. In addition, the analyzed device based on JL aspect exhibits a good reliability at short-circuit conditions. Moreover, the device breakdown voltage, specific on resistance and drain current are studied in order to reveal and provide some insights regarding the impact of design dimensions on these electrical performances. Besides, the output and transfer characteristics are compared to those of the conventional counterpart, as well as the critical electric field at breakdown. It is found that the proposed structure pave the way for achieving enhanced derived current capability, while maintaining excellent breakdown characteristics. These significant results makes the proposed JL structure a promising candidate toward the design of high-performance and cost-effective 4H-SiC MOSFETs, which are highly suitable for power electronics applications.*

2.1 Introduction

During the last few years, much effort has been devoted to address the tradeoff between the breakdown voltage and the specific on resistance in power devices, which constitutes the main problem for the design of high performance circuits [1-3]. In this context, SiC power MOSFET design technology is regarded as a prospective research area, where more perspectives for performances improvement are available [1-5]. For that reason, numerous device structures have been recently introduced. Mainly, the trench gate power MOSFET is one such type of power MOSFET encompassing multiple variants [2-6]. For instance, trench MOSFET with float islands or trench MOSFET with shielded regions or trench MOSFET with L-shaped p-substrate is investigated, where the main purpose is to solve the problem of high electric field at the edge of the gate oxide and modulate the electric field in the drift region [2-5]. Besides, super junction power MOSFETs has been recognized as the most important innovative idea enabling the opportunity to reach the main advantage of two dimensional coupling of the electric field [5]. Practically, as the p-n junction length increases it becomes two dimensional by inserting alternating pillars of p-type and n-type regions, which allows raising the drift region doping level and, accordingly, reducing its associate resistance while compensating the additional current [6]. Considerable modifications of the super junction power MOSFET design have been recently introduced and investigated in the literature [7-9]. Despite this, the elaboration of such complicated structures is considered challenging due to the high thermal budget and processing complexity required for the realization of abrupt junctions [10-13]. On the other hand, planar power MOSFET design is widely investigated, where several strategies such as the insertion of multi-section guard rings are investigated [13]. The latter strategy allows creating a uniform and flat distribution of the surface electric field, which can in turn enhance the device performance [10] and [12].

Basically, the specific resistance issue is regarded as the most pronounced problem in SiC-based power devices due to the low field effect mobility caused by the SiC/SiO_2 interface defects in the inversion layer [13]. Therefore, new design methodologies are urgently required to address the above-mentioned technological and performance challenges and to achieve high performance SiC-based power MOSFET devices. Intuitively, Junctionless (JL) aspect has demonstrated its ability for achieving the dual benefit of enhanced device performances and reduced elaboration cost in nanoscale MOSFETs [14-17].

To the best of our knowledge, no investigations have been carried out for enhancing the performance of 4H-SiC-based power MOSFET devices by using junctionless paradigm. In that perspective, the present work investigates the role of junctionless aspect in improving the performance of power MOSFET device. For this purpose, accurate numerical models are developed to analyze the electrical performances of the proposed device based on junctionless aspect. In addition, the critical electric field at the breakdown is analyzed, and the avalanche region is depicted. Furthermore, the drain current, the breakdown voltage, and the specific on resistance are studied with respect to variable dimensions of the trench oxide. It is revealed that the proposed structure not only allows reducing the specific on resistance, but also paves the road for reaching higher breakdown voltages. Therefore, the obtained results suggest that the investigated junctionless structure herein show a cost-effective approach for developing novel 4H-SiC power MOSFET structure potentially appropriate for high temperature and power applications.

2.2 Device structure and numerical modeling

In this section, we present our new proposed design, explain the drain current flow through the trench oxide, and give some clarifications about its fixed parts. Next, we discuss the numerical framework in terms of models and experimental data.

2.2.1 Device design

Fig.2.1 shows a cross sectional view of (a) the conventional planar power MOSFET and (b) the proposed junctionless Power MOSFET. The drift region is lightly doped with a uniform profile; the structure is symmetrical with an n-type polysilicon gate. Unlike the traditional structure, the proposed design consists of introducing a buried symmetrical oxide closed at the lateral edges of the device, to prevent current flow, and create two wells of semiconductor isolated from the direct contact with the drift region, with an opening on the gate side to allow current flow when the gate is correctly biased. The current flows to the drift region through a groove-like region characterized by two squared openings in different dimensions.

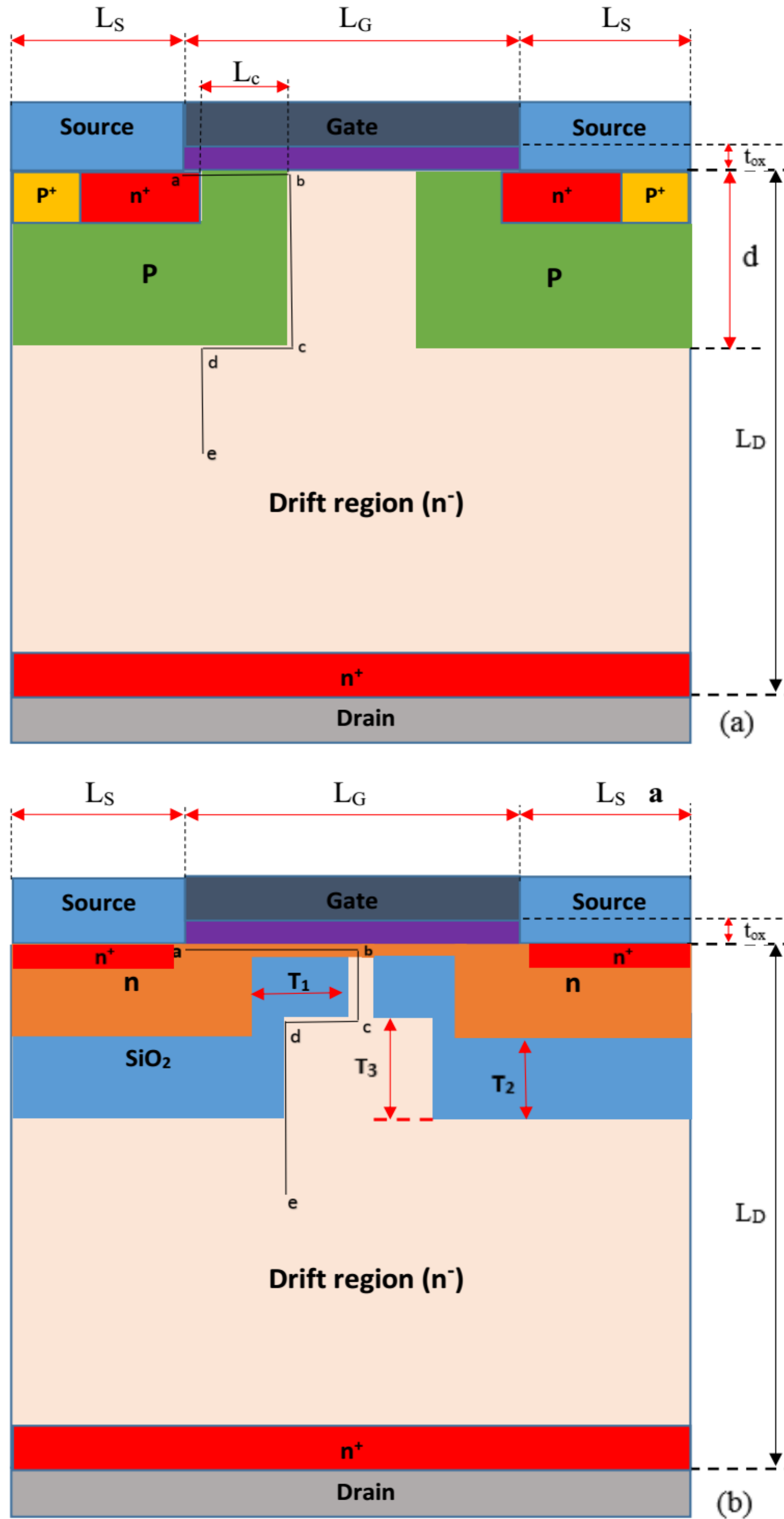


Figure 2.1 *Schematic of the cross sectional view of (a) the conventional planar power MOSFET; (b) the proposed junctionless power MOSFET.*

In this context, the upper one is taken as small as possible to preserve saturation, and the lower one is considered large to minimize the resistance. The doping concentration of the region located above the drift region and in between the two parts of the oxide is slightly higher than that of the drift region, and equal to the doping concentration of the regions delimited by the electrodes and the buried oxide, with a Gaussian doping profile. The main idea behind this new structure resides in the replacement of the p-substrate in the conventional design by a trench oxide. It is important to notice that similar design parameters are used for investigating both conventional planar power MOSFET and the proposed JL structure. Table.2.1 recapitulates various simulation parameters of both devices.

Table 2.1 *Simulation parameters of both the proposed device and its conventional counterpart.*

Parameter	Notation	Unit	Conventional Power MOSFET	proposed power MOSFET
Channel length	L_C	nm	1000	/
Source length	L_S	nm	999	999
Cell depth	L_D	nm	15000	15000
Gate length	L_G	nm	4000	4000
Thickness of the gate insulator	t_{ox}	nm	35	35
Doping concentration of P-substrate	P	cm^{-3}	10^{17}	/
Work function of the gate	ϕ_f	eV	4.63	4.63
Depth of P-substrate	d	nm	3500	/
Doping concentration of Source/drain regions	n^+	cm^{-3}	10^{18}	10^{18}
Doping concentration of the drift region.	N	cm^{-3}	10^{15}	10^{15}

2.2.2 Simulation models

As a matter of fact, the use of appropriate numerical models and fitted model parameters is indispensable for an accurate simulation; furthermore, no set of models is satisfying across all simulations in different conditions. In this work, it is important to point out that all simulations are conducted at temperature equals 300 K. Besides, since our contribution relies on a newly proposed

design, no calibration at the level of the device could be done owing to the lack of experimental data. However, experimental calibration of some parameters models could be achieved. In this context, the most important models included in all simulations are the mobility and generation/recombination models. In regard to mobility, parameters of the atlas models denoted: «Fldmob» and «analytic» of the high field dependent mobility and low field dependent mobility respectively, employed in this work are fitted from measured data given by [13]. The fldmob model describes the dependency of mobility on high electric fields involving drift velocity saturation, which is considered important for investigating power devices. Moreover, the analytical model takes into account temperature and doping effects for low field mobility [14]. The mobility model that takes into consideration the velocity saturation is given by the following equations

$$\mu_n(E) = \mu_{n0}\left[\frac{1}{1+\left(\frac{\mu_{n0}E}{V_{satn}}\right)^{\beta}}\right] \tag{2.1}$$

$$\mu_p(E) = \mu_{p0}\left[\frac{1}{1+\left(\frac{\mu_{p0}E}{V_{satp}}\right)^{\beta_p}}\right] \tag{2.2}$$

Where E denotes the electric field, V_{satn} and V_{satp} are the saturation velocities for electrons and holes, β_n and β_p are constants, and μ_{n0}, μ_{p0} are the electron and hole low field mobilities.

Concerning generation and recombination, the related atlas model used for simulations is the Shockely-Red-Hall model denoted «srh», which describes the effect of deep impurities on the device properties [18]. Parameters of this model are fitted based on experimental data given by [19], where the most important ones are electrons and holes lifetimes. To this extent, the latter parameters are used in the SRH recombination model, which can be described a function of impurity concentration using the following equation

$$R_{srh} = \frac{pn - n_i^2}{\tau_p\left[n + n_i \exp\left(\frac{E_{trap}}{KT_l}\right)\right] + \tau_n\left[p + n_i \exp\left(\frac{-E_{trap}}{KT_l}\right)\right]} \tag{2.3}$$

where n, p and ni are respectively the electron, hole and intrinsic concentrations, E_{TRAP} denotes the difference between the trap energy level and the intrinsic Fermi level, T_L is the lattice temperature, K refers to the Boltzmann constant, τ_n and τ_p represents the electron and hole lifetimes, respectively. The latter parameters are taken from the experimental results to be very close to the realistic behavior of the analyzed SiC power MOSFET device [19].

On the other hand, the breakdown simulation of power devices depends mainly on the impact ionization of electrons and holes as well as material crystallographic properties. Accordingly, the impact ionization model adopted in the device breakdown simulation is the model denoted «aniso» and the data are experimentally derived from the work carried out by [20]. The latter is appropriate for modeling SiC-based devices owing to its ability to take into account the anisotropic nature of SiC material. Accordingly, the electron and hole impact ionization rates, α_n and α_p which are necessary for the prediction of the device breakdown characteristics, are modeled though the following empirical expression

$$\alpha_{n,p} = \alpha_{0n,p} \exp\left(\frac{-b_{0n,p}}{E}\right) \tag{2.4}$$

Where, α_{0n}, α_{0p},$b_{0n}$and $b_{0p}$are parameters depending on the 4H-SiC material structural and crystallographic characteristics [20].

2.3. Results and discussion

In order to investigate the electrical characteristics of this new junctionless structure, a set of numerical simulations are established and discussed in this section.

2.3.1 Drain current

The output characteristics of both conventional and proposed 4H-SiC power MOSFET devices with and without JL aspect are depicted in Fig.2.2.

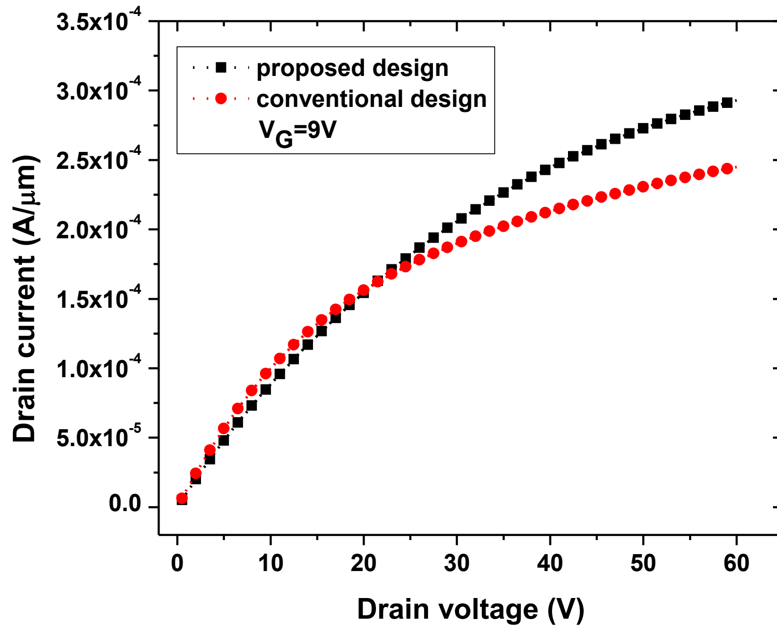


Figure 2.2 *Output characteristics (Ids-Vds curves) of both the proposed junctionless power MOSFET and its conventional counterpart.*

It can be observed from the latter figure that the proposed junctionless power MOSFET exhibits a validated semiconductor behavior with respect to its conventional counterpart. Specifically, an ohmic part for which the device behaves like a pure resistor crossed by a current, followed by a saturated region where the linearity of the relationship between the drain current and the drain voltage is not satisfied. In addition, in the ohmic part, it is noted that the drain currents of both the proposed device and its conventional counterpart are almost identical. However, the drain current of the proposed device becomes superior to that of the conventional one in the saturation part. This superiority can be attributed to the fact that the need for high inversion current is altered by the low mobility of the channel in the conventional case.

Numerous reliability shortcomings of Silicon Carbide have been linked to gate oxide for a long time since the introduction of SiC based power MOSFETs [21-23]. Among those problems, the threshold voltage instability has been widely recognized. In fact, drain current could be reduced due to threshold voltage positive shifts. To assess this effect, Fig.2.3 compares Transfer characteristic (I_{ds}-V_{gs}) of both the proposed junctionless power MOSFET, and its conventional counterpart.

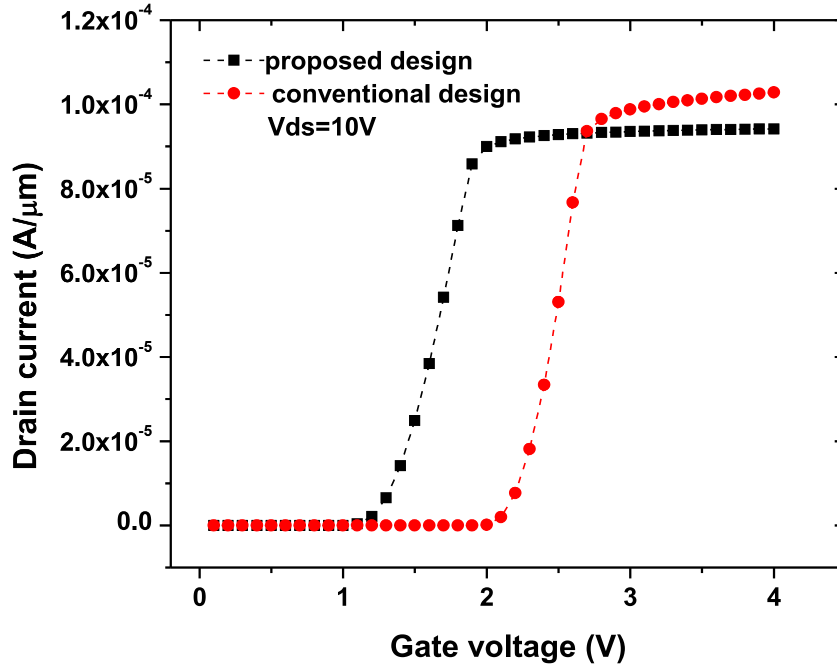
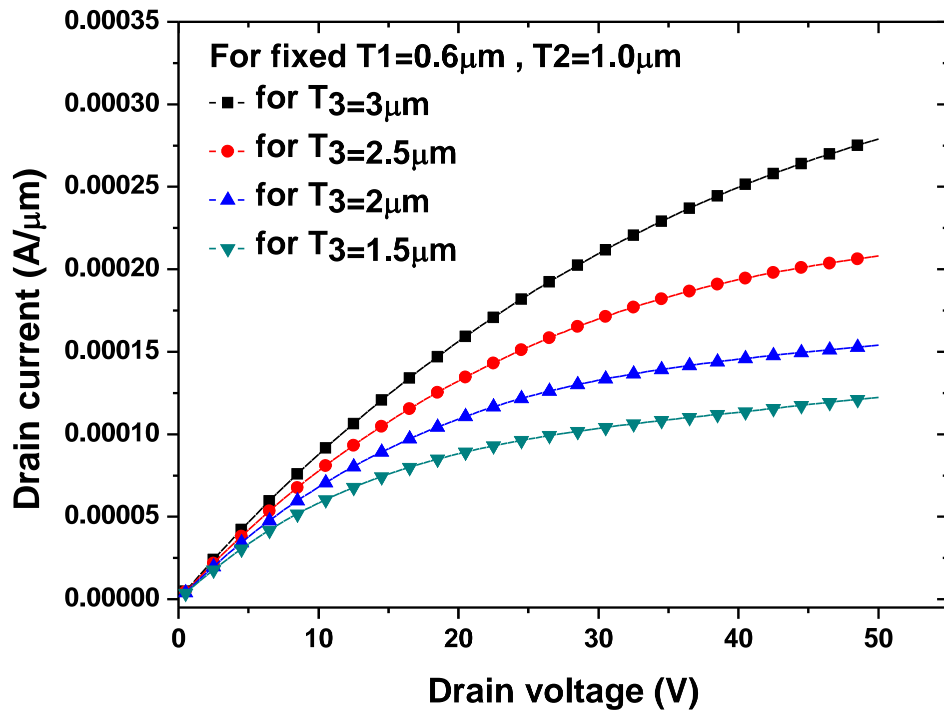


Figure 2.3 *Transfer characteristic (Ids-Vgs curves) of both the proposed junctionless power MOSFET, and its conventional counterpart.*

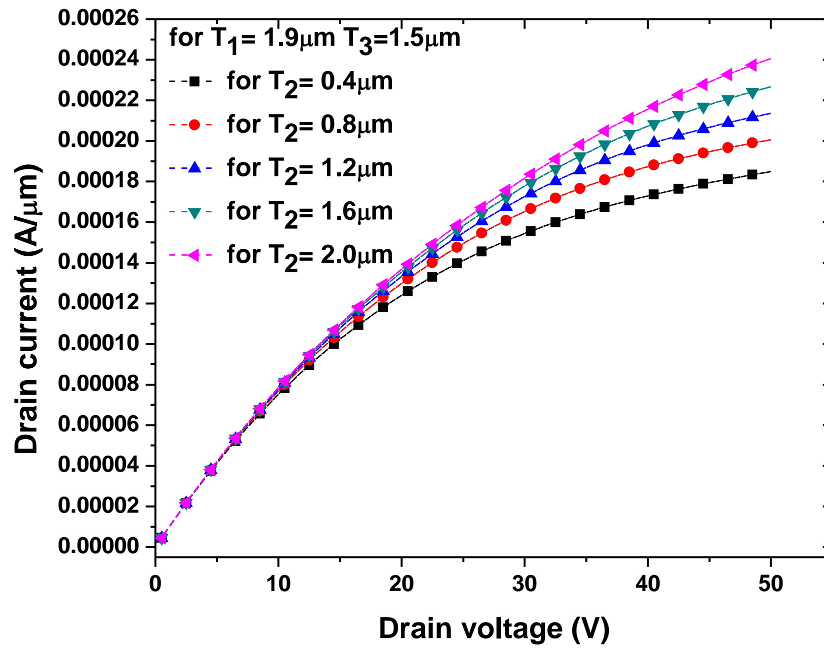
It is clear from the latter figure that the threshold voltage of the proposed design is smaller than that of the conventional structure by at least one order of magnitude (1.1 V, 2.2 V). Consequently, reducing the threshold voltage is attainable without the need for high k materials. Such a result can be perceived, otherwise, as a less stress (gate bias) on the gate oxide is needed to create the same drain current amplitude, which, over time, yields more reliability of the gate oxide. This can also lead to reduce the power consumption of the device, which is important for power electronics applications. Thereby, more stability and more sustainability at fabricant ratings of the threshold voltage and the drain current could be achieved. On the other hand, power loss is considered one of the most important parameter allowing the evaluation of power devices regarding energy dissipation properties. In this framework, the working power can be defined by $P= Ids \times Vds + Igs \times (Vgs + |Vgs - Vds|)$. The latter is calculated for both conventional and proposed devices. The obtained results indicate that the proposed JL device exhibits lower power value of 9×10^{-4} W as compared to that of the conventional structure ($P=13\times10^{-4}$ W) at Vds=20 V and Vgs=4 V. This emphasizes the low power consumption of the proposed device based on JL aspect. This

improvement concerning the device power consumption characteristics is attributed to the use of JL aspect, inducing significant changes in the device sub-threshold behavior as it is above-outlined. Intuitively, the geometry of the inserted trench oxide may influence the electrical properties of the proposed Junctionless 4H-SiC Power MOSFET. Accordingly, Fig.2.4 (a), (b) and (c) respectively present the impact of the trench oxide dimensions T_1, T_2, T_3, on the drain current. For all three structural parameters, T_1 has the more pronounced impact on the amplitude of the drain current; i.e. the drain current amplitude is ten times greater with a slight variation of T_1 less than 1 micron. On the other hand, when T_3 increases the drain current increases and thus lower on resistance can be achieved. It can be observed from Fig.2.4 (b) that the drain current increases proportionally without a noticeable saturation when T_2 increases. It is also clear from Fig.2.4 (c) that the variation of T_1 leads to significantly modulate the device resistive behavior, where the drain current increases exponentially with the T_1 increase. Moreover, it can be noticed that the drain current becomes more dependent to voltage fluctuation when T_1 increases, indicating its effect on the current saturation behavior of the Power MOSFET. In other words, the drain current is less saturated when T_1 increases. On the other hand, T_2 does not influence the drain current saturation behavior as can be disclosed from Fig.2.4 (b), where all drain current curves have the same shape in the saturation regime. For the third geometrical parameter of the introduced buried oxide (T_3), a minor impact on the drain current curves can be noted when T_3 increases with a more noticeable saturation region for low T_3 values. As a matter of fact, the conventional structure exhibits a complex electrical behavior, where it shows challenges concerning the saturation behavior.

In this context, the introduced oxide trench can influence greatly the electrical behavior of the investigated 4H SiC MOSFET, promoting enhanced saturation behavior. This benefit is considered highly suitable for analog and digital power electronic applications. Therefore, the saturation limitations associated with the conventional power MOSFET devices can be addressed by the proposed JL structure with oxide trench paradigm and further improvements can be achieved by optimizing the inserted trench oxide geometrical parameters.



(a)



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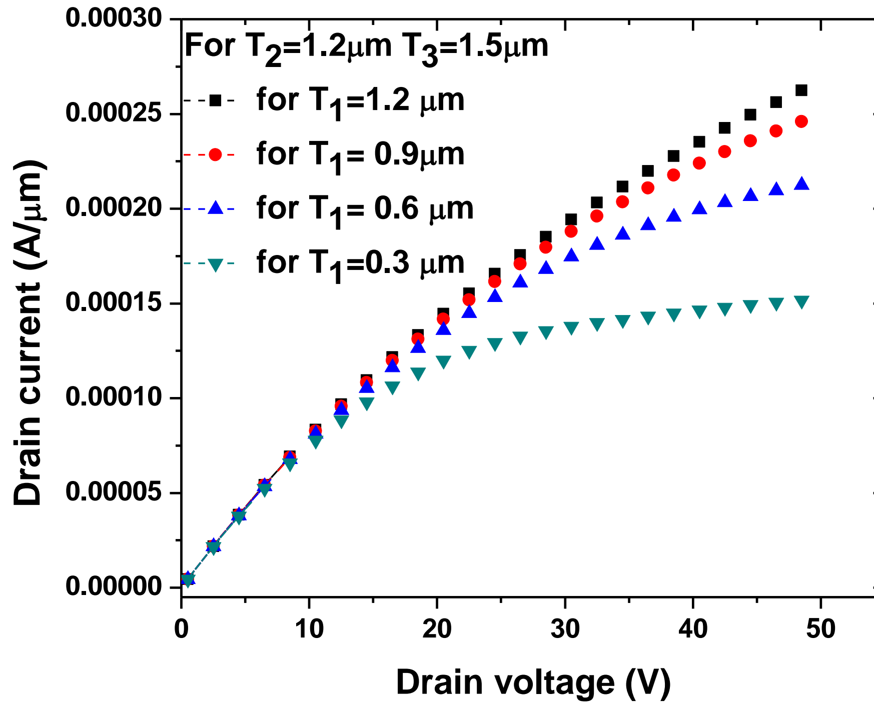


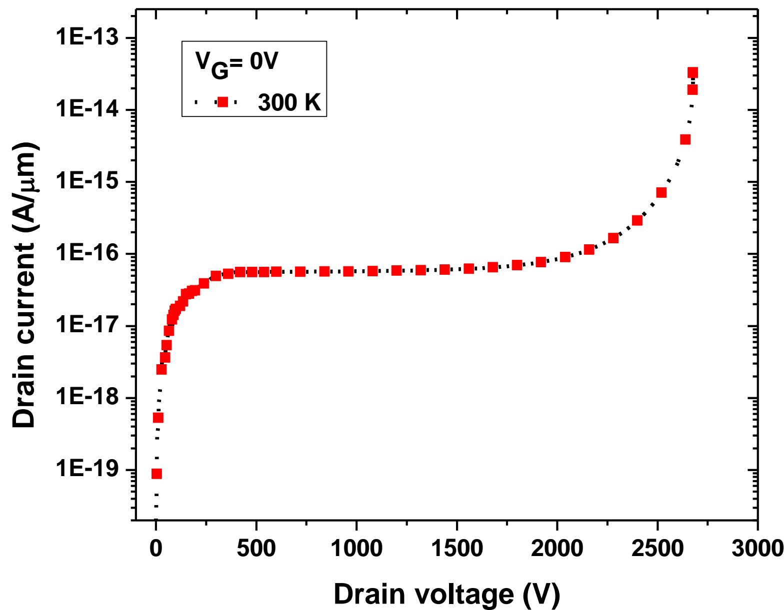
(c)

Figure.2.4 *Drain current of the proposed junctionless power MOSFET versus the drain voltage for different values of the geometrical parameters of the introduced oxide* ***(a)*** T_3*,* ***(b)*** T_2 *and* ***(c)*** T_1*.*

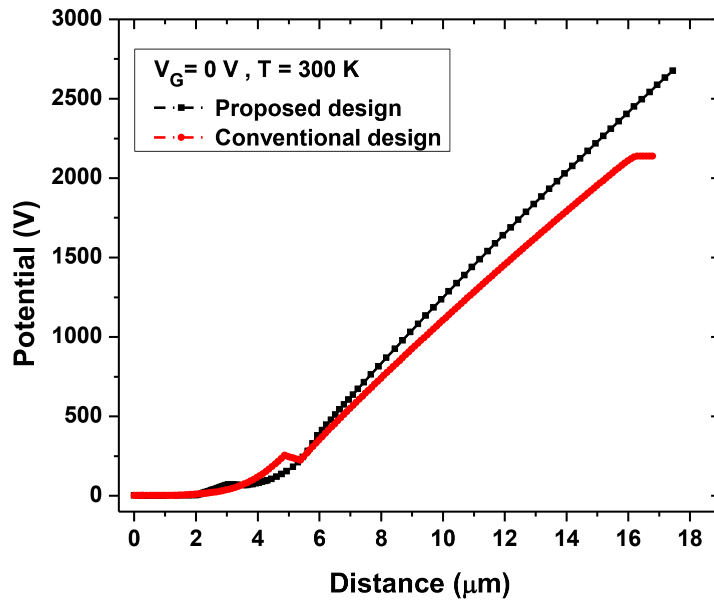
2.3.2 Breakdown simulation

Fig 2.5 (a) shows the breakdown characteristic of the proposed device during blocking mode, at room temperature and zero gate bias. The two basic parts of a breakdown characteristic can be recognized: the forward blocking part where the device does not lose its functional ability with a small leakage current. Besides, the second region presents the breakdown part where the device loses its functionality and, thereby, leads to induce significant damages. In order to get a profound insight regarding the breakdown properties of the investigated Power MOSFETs with and without Junctionless aspect, Fig. 2.5 (b) and (c) depict the plots of the potential and critical electric fields at breakdown condition, across cut-lines illustrated in Fig 2.1 by the path (a-b-c-d-e) of both the proposed device, and its conventional counterpart. It can be observed from the obtained distributions that both structures show the same profile. In the first 2.5 microns, the potentials and

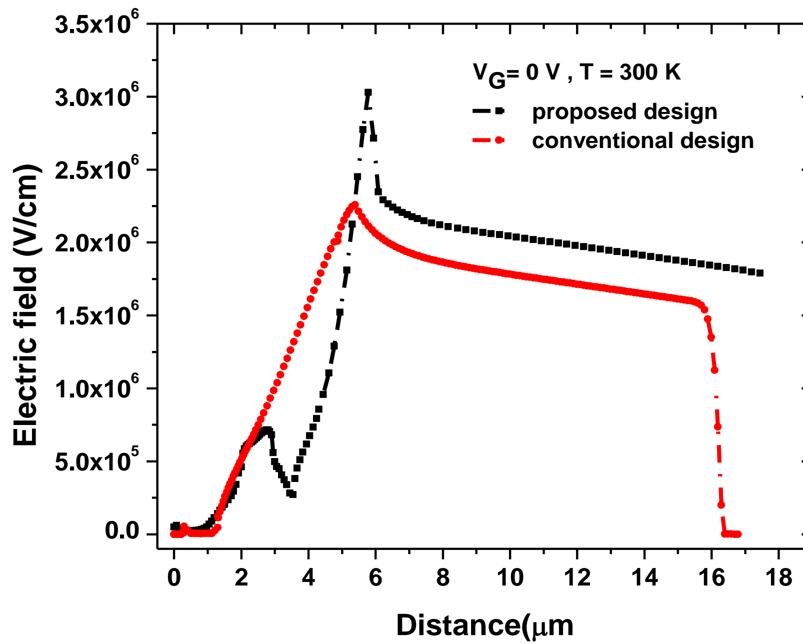
electric fields associated with the conventional and the proposed devices are equal. This distance represents the part at the vicinity of electrodes and the beginning of the drift region. However, the electric field of the proposed device decreases at the top of the larger groove of the trench oxide between c-d path, which is considered as a relaxation direction. The latter is inexistent in the conventional device. In the direction d-e, the electric field of the proposed device regains its increasing behavior. The associated electric field increases for both structures with and without junctionless aspect until reaching different maximum values. These high electric field values determinate the breakdown critical point for each device. As it is clear from Fig 2.5 (c), the critical point of the proposed device is higher than that of the conventional counterpart, namely 3.02×10^{6} V/cm for the new design, and 2.34×10^{6} V/cm for the conventional one. In this framework, Fig 2.5 (d) elucidates the critical electric field profile of the proposed device. It can be revealed from this figure that the breakdown region is located at the end of the trench oxide, whereas, the breakdown occurs at the junction between the P-substrate and the drift region for the conventional device. Therefore, it can be stated that the removal of the junction in our new Junctionless structure opens up new pathways to support higher electric fields compared to the conventional planar device.



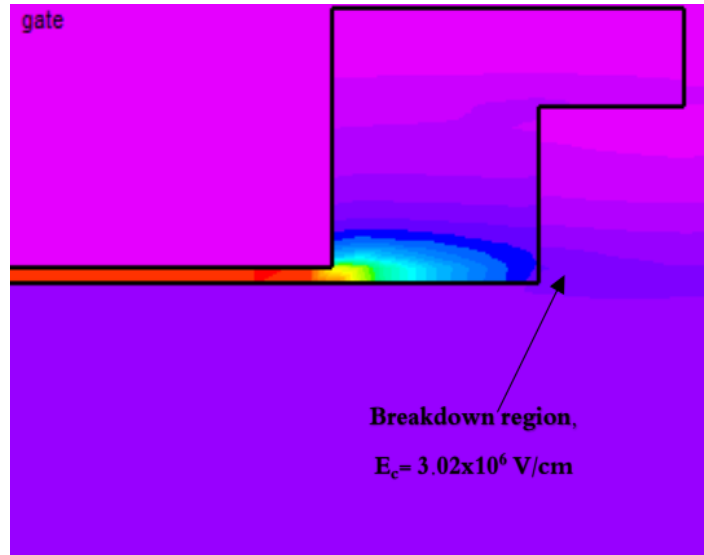
(a)



(b)



(c)



(d)

Figure 2.5 ***(a)*** *Breakdown characteristic of the proposed junctionless power MOSFET.**(b)**and **(c)** Potential and Electric field distributions at breakdown conditions across the cutline path of a-b-c-d-e for both the proposed junctionless power MOSFET and the conventional device. **(d)** The electric field profile at the breakdown region of the proposed junctionless power MOSFET.*

In order to investigate the switching characteristics of the proposed JL 4H-SiC power MOSFET device, Fig.2.6 shows the variation of the drain current as a function of the gate voltage for dissimilar drain voltage values. Besides, the associated swing factor for each configuration is extracted. It can be seen from the obtained I-V characteristics that the proposed device shows excellent switching properties, where the results demonstrate that a swing factor 62 mV/dec is achieved for Vds=2 V and a value of 64 mV/dec is reached for Vds=2 V. The obtained results indicate the high switching capabilities of the proposed device based on JL paradigm.

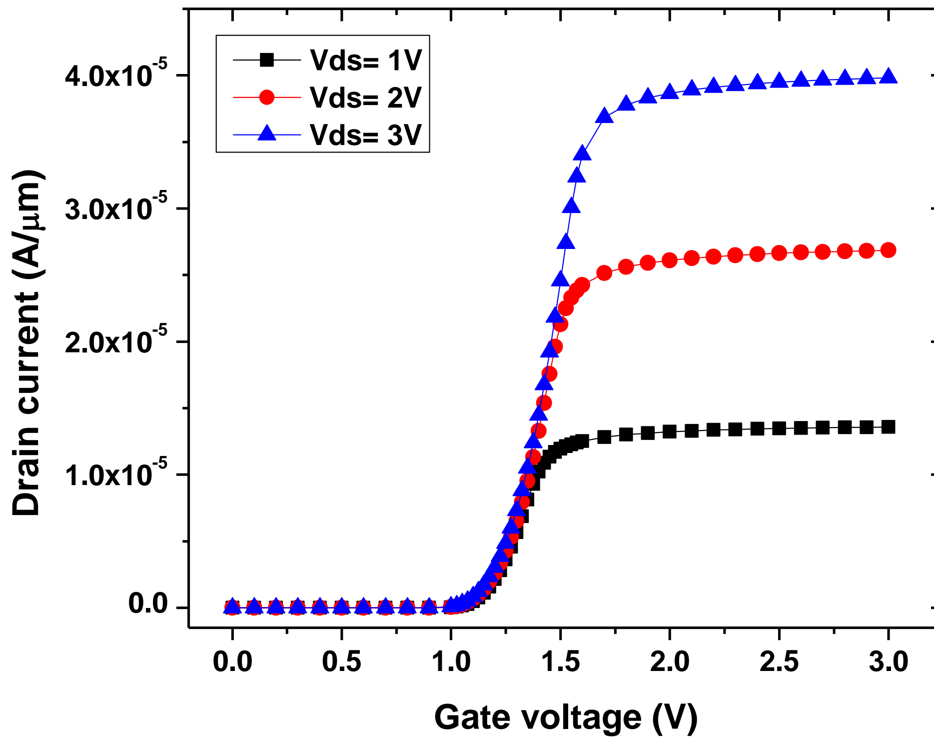
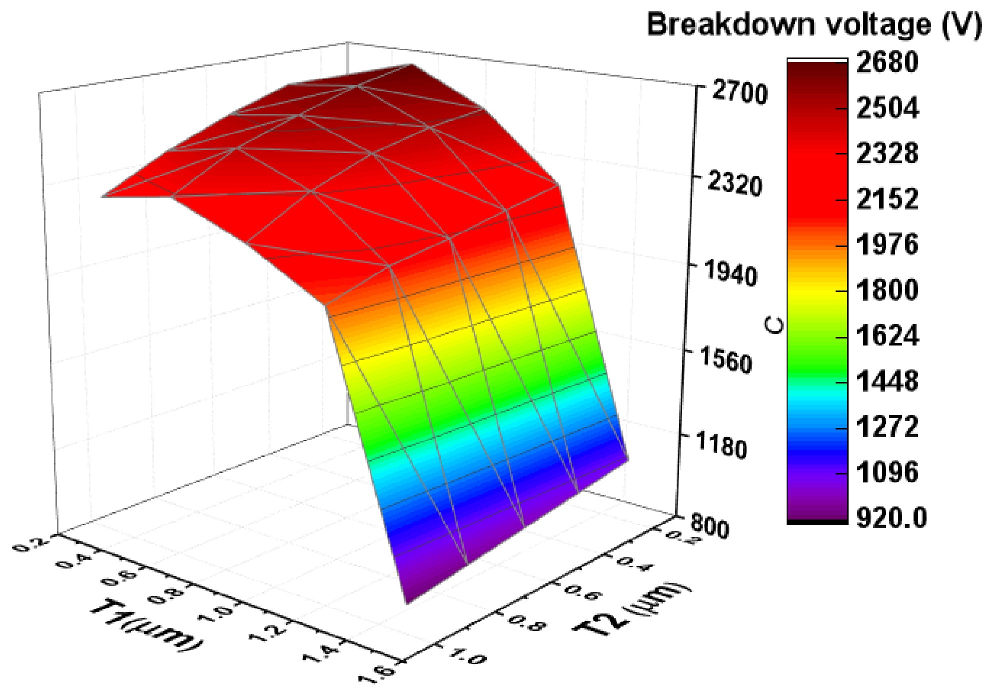
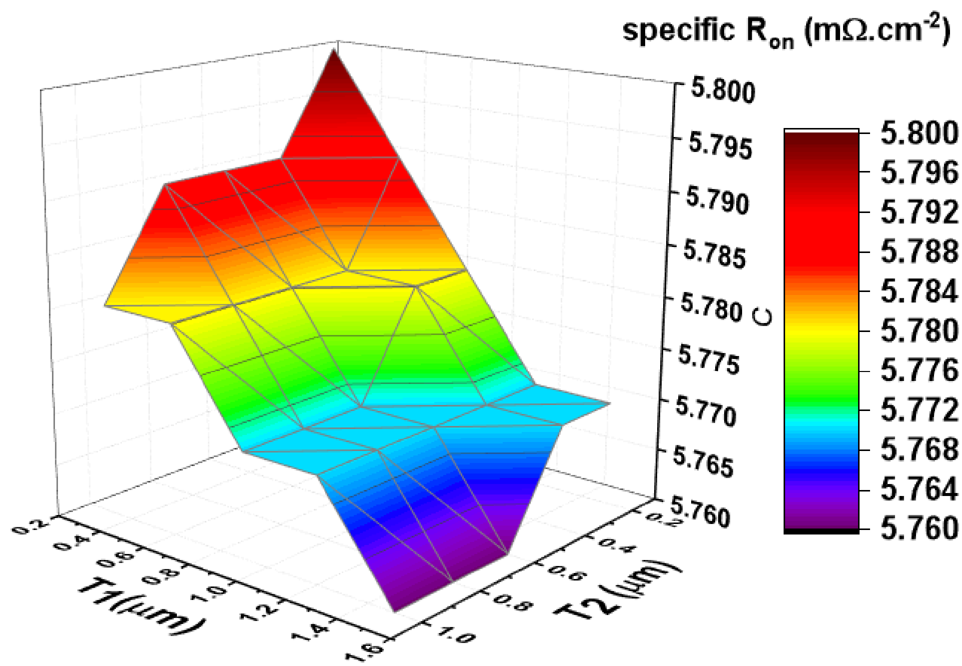


Figure 2.6 *Variation of the drain current as a function of the gate voltage for dissimilar drain voltage values.*

Aiming at investigating the impact of the inserted oxide geometry on the breakdown characteristics and on resistance of the investigated 4H-SiC JL Power MOSFET device, Fig 2.6 shows the variation of the breakdown voltage and the specific on resistance as a function of the trench oxide dimensions (T_1 and T_2). It can be seen from Fig.2.7 (a) that the breakdown voltage is inversely proportional to T_2 geometrical parameter. The same holds true for T_1 until an upper limit where the breakdown voltage starts decreasing as T_1 decreases. Regarding the specific on resistance values, it is clear from Fig 2.7 (b) that the variations of T_1 and T_2 parameters cannot affect the specific on resistance. This is mainly attributed to the role of the proposed JL structure in modulating the electric field distribution, thus leading to induce significant changes on the breakdown properties of the device.



(a)



(b)

Figure 2.7 ***(a)*** *Breakdown voltage and* ***(b)*** *on resistance of the proposed junctionless power MOSFET as a function of T_1 and T_2 dimensions of the buried oxide.*

In order to assess the performance of the proposed device structure based on JL aspect, Table 2.2 recapitulates performances of trench gate power MOSFETs, and our proposed junctionless planar power MOSFET in terms of breakdown voltages, specific on resistances, Baliga's figure of merit and elaboration cost. In this context, it can be concluded that the proposed device greatly outperforms all the trench gate devices in terms of breakdown characteristics. As for specific on resistance, our proposed device exhibits higher on-resistance compared to other devices. This is quite logical for planar devices as compared to trench-based structures, where the structure width is reduced by the insertion of the gate in the semiconductor to suppress the JFET region. However, a higher specific on-resistance is advantageous regarding reliability in blocking mode, when disrupted by contingent short-circuits. In those circumstances, a higher specific on resistance is required to limit the short-circuit current, and prevent the device damage. Such feature becomes a device quality when the device figure of merit is superior, which is the case in our proposed device. In fact, the figure of merit of our proposed device is higher than almost all trench gate power MOSFETs as it is emphasized in Table 2.2.

***Table 2.2** Performance comparison of the proposed 4H-SiC Power MOSFET based on JL aspect with the conventional devices.*

References	POWER MOSFETS	BV (V)	$R_{On,sp}$ (mΩ.cm^{-2})	FOM (V^2/ mΩ.cm^{-2})	Elaboration Cost
[2]	LSG-MOS	1230	6.39	236	High
[2]	DSS-MOS	1235	2.58	591	High
[2]	T-MOS	1295	1.95	860	High
[5]	Device A	1500	2.4	938	High
[5]	Device B	1560	2.02	1203	High
This work		2676	5.78	1236	Low

More importantly, the proposed design based on Junctionless technology is considered cost-effective as compared to other structures. This is due to its ability for avoiding the elaboration of costly abrupt-junctions. It should be noted that a planar structure lacks the two dimensional coupling of the electric field provided by the trench structure. Such situation limits the planar structure from surpassing the trench structure in terms of BFOM. These improvements in terms of breakdown characteristics demonstrate the beneficial role of the proposed JL structure for the

realization of high performance 4H-SiC Power MOSFETs using less processing complexity, a feature that is distinctively superior to conventional structures.

2.4 Conclusion

In this chapter, a novel planar power MOSFET based on the Junctionless concept has been proposed, investigated, and compared to its conventional counterpart, using accurate numerical models. It is found that the proposed structure exhibits an enhanced electrical behavior in high voltage biases as compared to the conventional one. This is attributed to the elimination of the hindering effect of the channel mobility. In addition, it is shown that the use of JL structure allows modulating device threshold characteristics, where the proposed JL device exhibits a lower threshold voltage of 1.1 V as compared to the conventional structure 2.2 V. The effect of the trench oxide dimensions on the drain current and breakdown characteristics has been carried out and thoroughly discussed. It is revealed that the proposed device demonstrates a great ability to support higher critical electric fields as compared to the conventional design, thus indicating its improved breakdown characteristics. These significant results makes the proposed JL structure a promising cost-effective strategy toward the design of high-performance 4H-SiC MOSFETs, which are highly suitable for power electronics applications.

2.5 References

[1] T. Muller, H. Nienhaus, "Ultrathin Ag films on H:Si(111)-191 surfaces deposited at low temperatures," J. Appl. Phys.,vol.93, pp.924–929, 2003.

[2] Gang Liu et al, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," Journal of applied physics, vol. 2, pp. 021307, 2015. ; doi: 10.1063/1.4922748.

[3] Yang et al, "4H-SiC Trench MOSFET with Splitting Double-Stacked Shielded Region," Superlattices and microstructures, vol. 122, pp. 419-425, 2018.

[4] Rakesh Vaid et al, "A novel trench gate floating islands power MOSFET (TG-FLIMOSFET):Two-dimensional simulation study". Microelectronic Engineering, 88, 11, 2011, 3316–3326.

[5] S. Hu et al. "A low specific on-resistance power trench MOSFET with a buried-interface-drain," Superlattices and Microstructures, vol. 85, pp. 133–138, 2015.

[6] H. Fu et al. "1200V 4H-SiC trench MOSFET with superior figure of merit and suppressed quasi-saturation effect," Microelectronics Reliability, vol. 123,pp. 114249, 2021.

[7] A. Testa et al, "Reliability of planar, Super-Junction and trench low voltage power MOSFETs," Microelectronics Reliability, vol. 50, pp. 1789–1795, 2010.

[8] H-S. Wang et al, "Ultra-low specific on-resistance 700V LDMOS with a buried super junction layer," Superlattices and Microstructures, vol. 113, pp. 478-482, 2018.

[9] Payal Nautiyal et al, "Performance evaluation of superjunction UMOS with dual polysilicon". Materials Today: Proceedings, 46, 10 (2021), 4546-4552.

[10] Wei Wu et al, "Low specific on-resistance power MOSFET with a surface improved super-junction layer". Superlattices and Microstructures, 72, 1–10, 2014.

[11] Xiaochuan Deng et al, "A robust and area-efficient guard ring edge termination technique for 4H-SiC power MOSFETs," Materials Science in Semiconductor Processing, vol. 68,pp.108–113, 2017.

[12] H. Ferhati, F. Douak and F. Djeffal, "Role of non-uniform channel doping in improving the nanoscale JL DG MOSFET reliability against the self-heating effects," Superlattices and Microstructures, vol. 109, pp. 869-879, 2017.

[13] Z. Bai et al, "Improving avalanche robustness of SiC MOSFETs by optimizing three-region P-well doping profile," Microelectronics Reliability, vol. 124, pp. 114332, 2021.

[14] V. Pavan Kumar Reddy et al, “Improved device characteristics obtained in 4H-SiC MOSFET using high-k dielectric stack with ultrathin SiO_2-AlN as interfacial layers,” Materials Science in Semiconductor Processing, vol. 80,pp. 24–30, 2018.

[15] H. Ferhati and F. Djeffal, “Graded channel doping junctionless MOSFET: a potential high performance and low power leakage device for nanoelectronic applications,” Journal of Computational Electronics, vol. 17, pp. 129-137, 2018.

[16] J.-P. Colinge et al., “Nanowire transistors without junctions,” Nature Nanotechnol., vol. 5, pp. 225–229, 2010.

[17] H. Ferhati and F. Djeffal, “Planar junctionless phototransistor: A potential high-performance and low-cost device for optical-communications,” Optics & Laser Technology, vol.97, pp.29-35, 2017.

[18] F. Djeffal, T. Bentrcia, M. A. Abdi and T. Bendib, “Drain current model for undoped Gate Stack Double Gate (GSDG) MOSFETs including the hot-carrier degradation effects,” Microelectronics Reliability, vol. 51, pp. 550-555, 2011.

[19] ATLAS user manual: Device simulation software, 2012.

[20] M. J. Marinella et al, “Carrier Generation Lifetimes in 4H-SiC MOS Capacitors,” IEEE Trans, Electron Devices, vol. 57, pp. 1910-1923, 2010.

[21] T. Hatakeyama et al, “Impact ionization coefficients of silicon carbide,” Appl. Phys. Lett., vol. 85, pp.1380, 2004.

[22] A. J. Lelis, R. Green and D. B. Habersat, “SiC MOSFET reliability and implications for qualification testing,”2017 IEEE International Reliability Physics Symposium (IRPS), pp. 2A-4.1-2A-4.4, 2017.

[23] B. Zerroumda, F. Djeffal, T. Bentrcia, H. Ferhati, “Numerical Analysis of 4H-SiC MOSFET Design Including High-k Gate Dielectrics for Power electronic Applications,”ACM-ICSENT 2018 Proceedings of the 7th International Conference on Software Engineering and New Technologies At: Hammamet, Tunisia — December 26-28, pp. 1–5, 2018.

[24] A. J. Lelis, R. Green, D. B. Habersat and M. El, “Basic Mechanisms of Threshold-Voltage Instability and Implications for Reliability Testing of SiC MOSFETs,” in IEEE Transactions on Electron Devices, vol. 62, pp. 316-323, 2015.

Chapter 3

A novel high-performance junctionless 4H-SiC trench MOSFET with improved switching characteristics

Abstract- *A high-performance novel 4H-SiC trench power MOSFET employing the junctionless concept is proposed in this chapter. The presented design is modeled and investigated numerically by Devedit and Atlas TCAD tools, where the advantages of the junctionless concept are used to maximize the performance of the trench structure. This new structure helps lowering the input and reverse transfer capacitances of the trench power MOSFET compared to the conventional structures. The proposed device shows a lower high frequency (HF) FoM value of 1078 mΩ.pF as compared to the conventional counterpart (4600 mΩ.pF), with a relative improvement of 76.5 %. Moreover, a superior agreement between the breakdown voltage and the specific on-resistance has been revealed by a higher Figure-of-Merit (BV2/Ron= 2580 MV/mΩ.cm-2) in comparison to recently published high-performing power MOSFETs. In addition, the proposed design proves to support a higher critical electric field at the gate edge in comparison to that of its conventional counterpart. The substantial outcomes of this study pairing improvements in switching, blocking and conducting electrical performances, forcefully suggest this cost-effective design as a potential candidate in developing low-cost and high-performance 4H-SiC power MOSFETS.*

3.1 Introduction

Nowadays, power electronic devices play a crucial role in developing modern electrical systems such as power energy converters, motor drives, electric vehicles, and power grids [1-5]. Power transistors are considered among the most competitive power devices since they are capable of delivering high drive current and fast switching speeds [1-5]. The emergence of power CMOS compatible technologies based on wide band-gap semiconductors opened new pathways for the development of power MOSFETs, offering high breakdown voltages, fast commutation speeds and low on-resistance which make them well suited for use in high-power applications [5]. Moreover, several design strategies such as trench gate power MOSFET, trench MOSFET with float islands, trench MOSFET with L-shaped p-substrate, super junction power MOSFET and optimized fabrication conditions have enabled a great promise to achieve important improvements in their thermal and electrical performances [3-8]. Despite these excellent capabilities, the use of wide band-gap critical raw materials (CRM) as well as high toxicity and expensive elements limited the mass production of GaN, InGaAs and Diamond-based power MOSFETs, where the production process of diamond films is still relatively expensive compared to other wide-bandgap materials such as SiC and GaN [9-11]. Alternatively, much research efforts have been devoted to Silicon and Silicon carbide (SiC) as promising CRM-free non-toxic, and cost-effective compounds for power electronics applications [1-8]. In this context, SiC-based power MOSFET is attracting considerable research attention due to their superb electrical and thermal properties, which results in improved overall performance and efficiency [1-8]. However, the switching speed/losses and specific On-resistance issues are regarded as the most pronounced problems in SiC-based power MOSFETs due to the high input and reverse transfer capacitances and the low electron mobility caused by the SiC/SiO2 interface low quality [12-14]. Therefore, new design strategies are required to address the above-mentioned limitations in order to achieve high-performance SiC-based power MOSFET structures. Accordingly, several device designs have been recently proposed. The trench-gate strategy is initially proposed, both to reduce the specific ON-resistance by the omission of the Junction-FET resistance, and to increase the breakdown voltage by the two dimensional coupling of the electric field. However, several challenges inherent to the trench gate structure have been emerged and led to further improvements of this structure; such as the insertion of an L-shaped p-substrate to overcome the challenge of high electric field at the edge of the gate

oxide and improve the electric field distribution in the drift region [3-5]. Super Junction (SJ) power MOSFET structure can further reduce the drift resistance by implementing alternating pillars of P-N junctions to allow increasing the drift region doping while maintaining a high breakdown voltage owing to the extension of the junction [6-8]. Complex and considerable design modifications of the trench gate and super junction power MOSFETs were recently proposed and analyzed to investigate the electrodes coupling effects, yet causing a significant increase in conventional structure capacitances leading to degraded switching characteristics [3-8]. Moreover, the fabrication of such complicated structures requires high thermal budget and complex elaboration processes for the realization of abrupt P-N junctions [3-8]. The fabrication of these abrupt junctions at high temperatures allow contaminated charge carriers to flow from source to channel and channel to drain [15]. This issue can be resolved by using the junctionless (JL) aspect [15-18].

Basically, the specific ON-resistance/breakdown voltage compromise and degraded switching characteristics issues are regarded as the most pronounced challenges in developing high-performance SiC-based power MOSFETs [13]. Motivated by these challenges, in the present chapter we investigate a new junctionless 4H-SiC trench MOSFET based on combining the junctionless aspect and improved gate trench MOSFET structure to bridge the gap between low cost elaboration processes and improved electrical and thermal characteristics. The proposed structure demonstrates very encouraging results in both switching and analog applications, as it combines the benefits of the junctionless technology and gate trench-based MOSFET design. Moreover, this new power MOSFET design opens up the path towards a generation of devices circumventing high-cost elaboration processes and promoting improved Figures-of-Merit (FoMs), making it both suitable and promising alternative for power electronics applications.

3.2 Device structure and Modeling frameworks

Fig.1 illustrates a cross sectional view of (a) the proposed JL and (b) the conventional trench SiC-based power MOSFETs. The main idea behind the proposed power MOSFET design is to consider a JL structure. For this purpose, the interface between the drain and the source preventing current flow is changed from a P-N junction structure to a simple buried oxide. Moreover, the concept of the created channel in the p-base region to allow the current flow is replaced by a new conduction path between source/gate and the buried oxide. In this framework, to avoid current flow between

the device lateral edges, we introduced a buried symmetrical oxide adjacent to the n-type body regions. The inserted buried oxide regions have the form of wells of semiconductor, isolating the drift region from body layers. Besides, an opening on the gate side is considered in the proposed JL structure to enable a conduction path ones the gate is properly biased. The introduced oxide regions are shaped following a grooves-like structure to preserve saturation, while maintaining low resistance. The drift region is suggested with a uniform n-type lightly doped profile. Whereas, the doping level of the layers between the gate oxide and the inserted grooves-like oxide regions is considered slightly higher than that of the drift region. Previously, we have considered a junctionless planar gate structure [14], where the reduction of the buried oxide depth is limited to maintain the saturation. However, in the junctionless trench gate structure the buried oxide depth can be reduced more, following the gate depth without losing saturation. The adopted design parameters for the numerical investigation of the proposed JL trench SiC-based power MOSFET are summarized in Table 3.1, where similar device configurations are used for investigating both proposed and conventional structures.

Table 3.1 *Simulation parameters of both the proposed device and its conventional counterpart.*

Parameter	*Notation*	*Unit*	*Conventional Power MOSFET*	*Proposed power MOSFET*
P region depth	L_C	nm	1000	/
Source length	L_S	nm	3000	3000
Cell depth	L_D	nm	15000	15000
Gate length	L_G	nm	80	80
Thickness of the gate insulator	t_{ox}	nm	40	40
Doping concentration of P-substrate	P	cm^{-3}	10^{17}	/
Work function of the gate	ϕ_f	eV	4.63	4.63
Depth of P-substrate	D	nm	1000	/
Doping concentration of Source/drain regions.	n^+	cm^{-3}	10^{18}	10^{18}
Doping concentration of the drift region.	N	cm^{-3}	6.5×10^{15}	6.5×10^{15}

It is important to note that the introduced buried oxide regions are characterized by two geometrical parameters namely T_1 and T_2 as it is shown in Fig.3.1 (a). These geometrical parameters can influence the device performance since they determinate the conduction path dimensions.

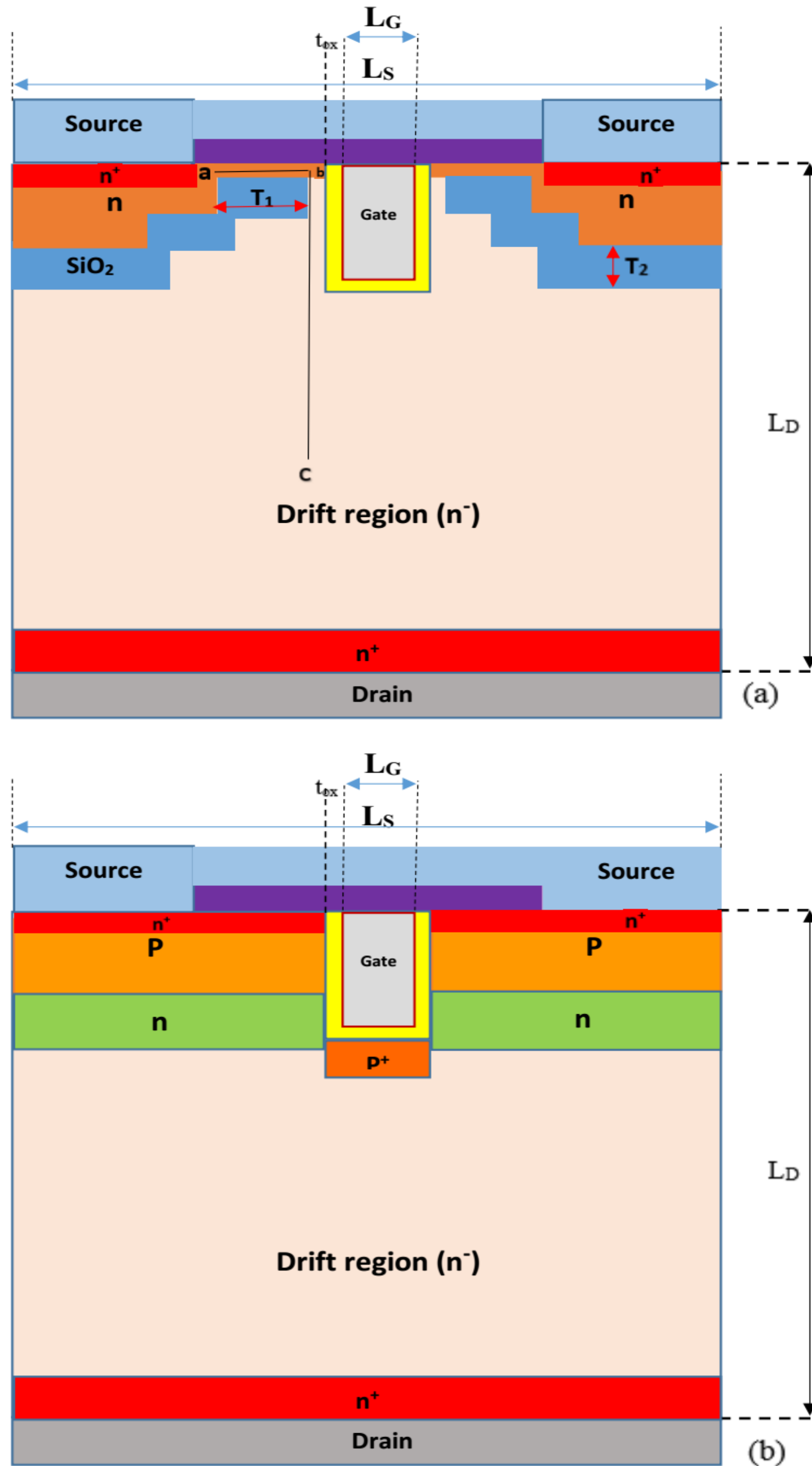


Figure 3.1 *Schematic of the cross sectional view of (a) the proposed junctionless trench power MOSFET; (b) a conventional trench power MOSFET.*

As a matter of fact, numerical tools are extremely important for the assessment of devices with innovative structure engineering aspects. This is mainly due to the ability of these tools for offering the possibility of predicting the device performance and optimizing the device structure without the need for highly expensive experimental path [16-19]. Following this direction, numerical models based on 2-D ATLAS module within SILVACO TCAD commercial software are used to evaluate the proposed JL trench power SiC-based MOSFET device regarding breakdown and switching characteristics for power electronics applications [20]. Before this step, the proposed structure consists of inserting symmetrical oxide regions as it is shown in Fig.3.1 (a). These oxide regions are shaped using a grooves-like structure to achieve a low R_{on} and reduced gate to drain capacitance. To do so, it seems essential to introduce these oxide regions using Devedit module available in SLVACO TCAD software. This tool allows simulating the elaboration of extremely complex geometrical structure. The simulations of the device performance are carried out within ATLAS module at room temperature conditions. To this extent, several mobility and generation/recombination models are included. Accordingly, «Fldmob» model denoting high field dependent mobility is considered in breakdown simulations, to take into consideration the impact of high electric fields on carrier mobility [12]. This effect is essential for the accurate modeling of power devices. Besides, «analytic» model describing low field dependent mobility is included to assess the influence of temperature and doping concentration on the low field mobility [16]. In addition, «srh» acronym denoting the Shockely-Red-Hall model is introduced to consider the impact of deep impurities on the device characteristics [20]. The electron and hole lifetimes (τ_n and τ_p) are taken from experimental data given in [21]. The SRH recombination model can be given by the following equation

$$R_{srh} = \frac{pn - n_i^2}{\tau_p \left[n + n_i \exp\left(\frac{E_{trap}}{KT_l} \right) \right] + \tau_n \left[p + n_i \exp\left(\frac{-E_{trap}}{KT_l} \right) \right]} \qquad (3.1)$$

where n, p and n_i refer respectively to the electron, hole and intrinsic concentrations, K is the Boltzmann constant, E_{TRAP} represents the energy difference between the trap level and the intrinsic Fermi level, T_L refers to the lattice temperature [21].

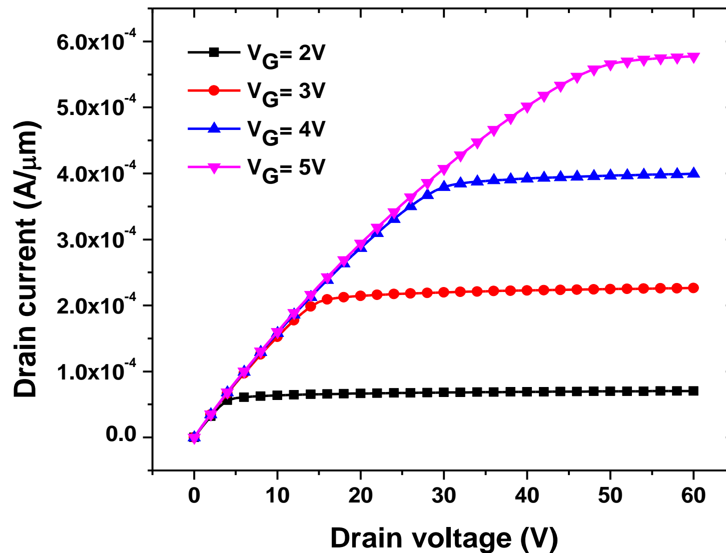
As for the device breakdown simulation, it is carried out by incorporating «aniso» model in which experimental data provided in [22] are used. This model is considered effective in modeling the SiC-based devices, being able to account for the anisotropic nature of SiC material. In this model, the impact ionization rates associated with electrons and holes are given in both parallel and perpendicular directions by the following empirical expression:

$$\alpha_{n,p} = \alpha_{0n,p} \exp\left(\frac{-b_{0n,p}}{E}\right) \tag{3.2}$$

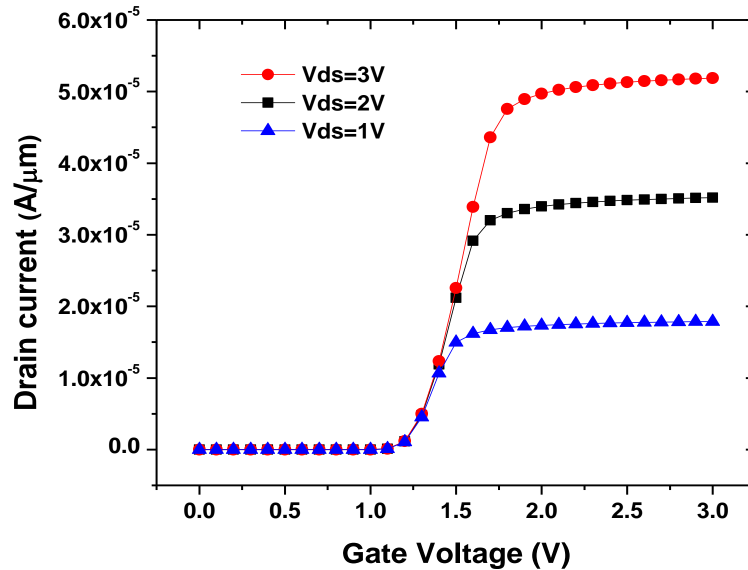
Where, α_{0n}, α_{0p}, b_{0n} and b_{0p} are parameters depending on the 4H-SiC material structural and crystallographic characteristics [22].

3.3 Results and discussion

Fig.3.2 shows I_{ds}-V_{ds} characteristics of the proposed trench power SiC MOSFET based on JL aspect for dissimilar applied gate voltages of 2V, 3V, 4V and 5V. It can be seen from Fig.3.2 (a) that the proposed device based on JL paradigm shows a semiconductor device behavior, namely: two working regimes. Particularly, we can notice an ohmic part, where the investigated power MOSFET works as a resistor with a linear tendency of the drain current with respect to the applied voltage, while it can be seen that further increasing of the drain bias leads to a near-perfect saturation.



(a)



(b)

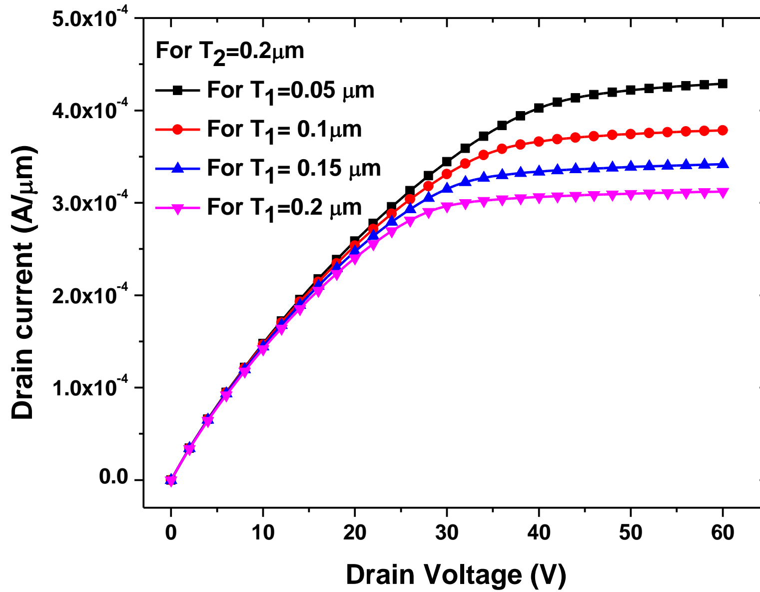
Figure 3.2 *(a) Variation of drain current as function of applied drain voltage for different gate voltages. (b) I_{ds}-V_{gs} characteristics of the investigated devices for dissimilar applied drain voltages.*

Besides, it can be observed from this figure that by increasing the gate voltage, the derived current capability increases. This can be explained by the increase of the accumulation charge in the opening between the gate and the trench oxide of the JL structure, thus leading to create a conduction path towards the drift region. Fig.3.2 (b) illustrates I_{ds}-V_{gs} curves of the proposed SiC power MOSFET device based on combined trench and JL aspects for various applied drain voltages. It is demonstrated from the latter figure that the proposed device exhibits a low threshold voltage of 1.2 V as compared to the conventional ones based on several structures [23]. This can in turn promote enhanced reliability of the SiC power MOSFET devices. In other words, the use of JL aspect can enable reducing the applied gate voltage (gate stress) required for achieving a favorable drain current, which leads to enhance the device reliability performances. This is mainly attributed to its enhanced subthreshold behavior, where the accumulation of conducting charges at the interface between the semiconductor and the gate insulator is not generated through inversion process, and not preceded by a partial depletion, rather it is a weak accumulation followed by a strong electrons accumulation at the threshold voltage condition, because only one type of majority

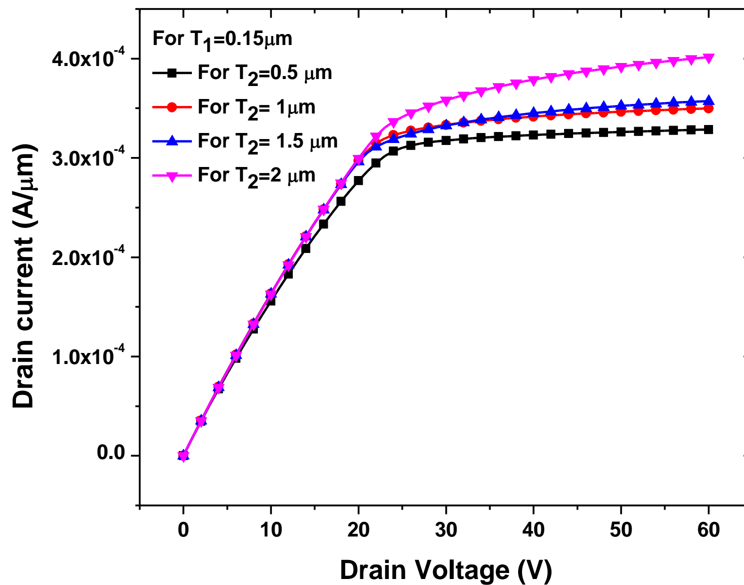
carriers is present in the entire device, and the gate is made of polysilicon doped with the same dopant type as the semiconductor. Therefore, the MOS structure causes accumulation in the semiconductor side. In fact, the gate stress can cause oxide damages, affecting the device threshold voltage stability and increasing power dissipation effects [24-26]. These issues are not pronounced for the proposed device owing to the use of JL technology, offering a low threshold voltage and less gate stress. Moreover, the device demonstrates an ultralow OFF-state current value of 5×10^{-16} A/µm^2. This is particularly due to the use of JL aspect combined with trench-based engineered structure, paving the way for nearing a theoretical zero current off-state in SiC-based power MOSFETs. This can in turn prevent carrier transfer to the drift region even when high drain voltages are applied. This benefit can reduce enormously the device power consumption, which is considered as a big issue in power electronic systems [23-27]. More importantly, the use of a JL structure for SiC trench power MOSFET devices can provide more sustainability from the device fabrication viewpoint, where reduced manufacturing processes thermal budget can be achieved by avoiding abrupt PN junctions.

To design a SiC trench power MOSFET based on JL technology, symmetrical grooves-like oxide layers are introduced to replace body regions as it is shown in Fig.3.1 (a). The geometry of the inserted trench oxide namely T_1 and T_2 dimensions can greatly influence the device performances. Thus, it seems important to study the effect of the oxide geometry on the device transfer characteristics. In this context, Fig.3 (a) and (b) show respectively I_{ds}-V_{ds} characteristics of the proposed SiC power MOSFET based on combined trench and JL structure engineering for various oxide dimensions T_1 and T_2. Observing Fig.3.3 (a), we can notice that the derived current capability of the proposed device is decreased by increasing T_1, where lower drain current values are noticed for T_1=200 nm. Moreover, it can be seen from Fig.3.3 (a) that drain current becomes less dependent to voltage fluctuation when T_1 increases, indicating its effect on the device current saturation behavior. Basically, increasing T_1 leads to lowering the amount of available charges that can participate in the conduction by enlarging the trench oxide towards the source side without affecting the saturation behavior, i.e. the same behavior is repeated with fewer amounts of charges, which is important in reducing the saturation current. On the other hand, a minor impact on the device derived current capability is observed for T_2 variation as it is illustrated in Fig.3.3 (b), where the drain current is slightly improved in the saturation region for higher values of T_2. It can be also demonstrated from the extracted I_{ds}-V_{ds} characteristics that the proposed device based on combined

trench engineering and JL technology offers improved saturation characteristics as compared to the conventional device [14, 23], even when changing the inserted grooves-like geometry. This behavior can be beneficial for analog and digital power electronic applications.



(a)



(b)

Figure 3.3 *I_{ds}-V_{ds} characteristics of the proposed device for (a) different T_1 oxide dimensions with T_2=0.2 μm (b) various T_2 oxide dimensions with T_1=0.15 μm.*

3.3.2 Switching simulation

As a matter of fact, energy loss appears from two dissimilar sources; the first one is related to conduction mechanism and extremely low ON-resistance (Ron) is required, while the second one is linked to the device switching characteristics. In this framework, the energy loss originates from charging and discharging of the gate capacitance during the device switching from ON to OFF states. To the best of our knowledge, these energy loss mechanisms are interlinked, where reducing Ron could result in poor switching characteristics of the device. With the aim of assessing the ability of the proposed SiC power MOSFET based on combined gate-trench engineering and JL structure to enhance the trade-off between energy loss and switching properties associated with the conventional device, we extracted Ron, input and reverse transfer capacitances (C_{iss} and C_{rss}) of both the conventional and the proposed devices. The latter capacitances are calculated using the following expressions

$$\begin{cases} C_{iss} = C_{gd} + C_{gs} \\ C_{rss} = C_{gd} \end{cases} \tag{3.3}$$

The extracted C_{iss} values as a function of the drain voltage for both conventional and proposed JL and conventional SiC gate-trench power MOSFET designs are depicted in Fig 3.4.

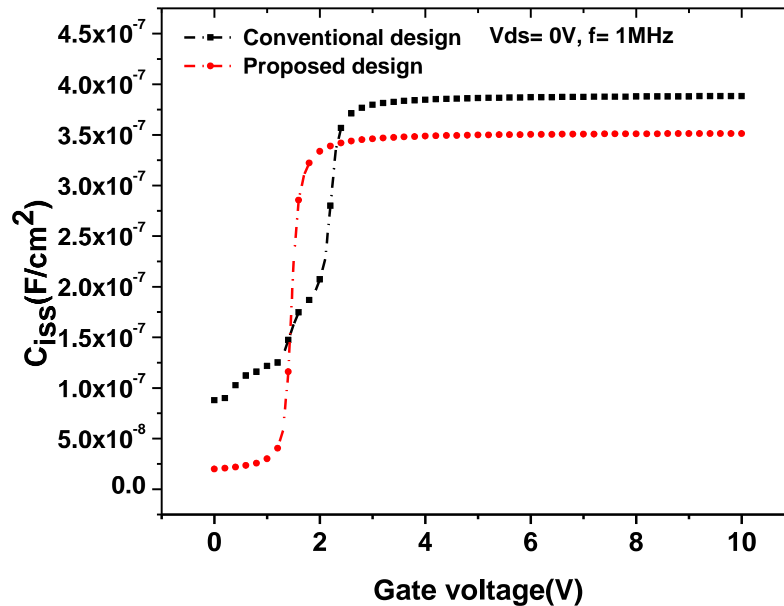


Figure 3.4 *Variation of the input capacitance as a function of gate voltage.*

It can be seen from this figure that the proposed device based on combined trench structure and JL structure can offer lower input capacitance values over a large drain operating voltage range. This indicates the propensity of the proposed device to improve the gate switching speed as compared to its conventional counterpart. This enhancement is mainly attributed to the role of using JL aspect in reducing the gate capacitance. Basically, we can improve the input capacitance either by expanding the depletion region which is the case in trench gate structures with super junctions, or by easing the onset of conduction by the gate which is the case in junctionless trench gate structures. On the other hand, the calculated Ron values for both conventional and proposed JL SiC trench power MOSFET devices are 2.09 $m\Omega.cm^{-2}$ and 1.61 $m\Omega.cm^{-2}$, respectively. This demonstrates the ability of the proposed device for achieving a lower ON-resistance value. This is mainly correlated with the role of using JL structure in reducing the spreading resistance due to the increased accumulation layer area. Besides, the use of trench engineered structure plays a crucial role in getting rid of parasitic JFET region, thus contributing to Ron reduction. Therefore, combining both trench structure and JL paradigm can provide new routes for addressing the trade-off between conduction and switching losses.

Fig.3.5 shows the variation of the reverse transfer capacitance versus the applied drain voltage for both investigated SiC trench power MOSFET designs with and without JL aspect. This figure confirms the improved switching losses of the proposed device with JL structure, where lower gate to drain capacitance values are achieved as compared to the conventional SiC trench power MOSFET device. This improvement can be explained by the fact that a smaller amount of charges compared to the conventional counterpart is required to generate the same conduction process in the junctionless device. Indeed, the improvement of the reverse transfer capacitance by the extension of the junction, results in a lower capacitance, but at the cost of being at higher values for lower drain voltages compared to the conventional case, and then decreasing below the conventional values with drain voltage increase, to regain the same values at elevated drain voltages [23]. Whereas, in the junctionless case, the reverse transfer capacitance is lower than that of the conventional counterpart across the board as can be observed from Fig.3.5.

On the other hand, an effective enhancement in SiC power MOSFET performance is achieved only if the product of Ron and gate to drain capacitance is reduced. To this extent, $Ron \times C_{rss}$ ($m\Omega.pF$) is called high frequency figure of merit (HF-FoM) that characterizes the device performance regarding several criteria. The proposed device shows a lower HF-FoM value of 1078 $m\Omega.pF$ as

compared to the conventional counterpart (4600 mΩ.pF), with a relative improvement of 76.5 %. These outstanding results prove the appropriateness of the JL aspect combined with gate trench engineering for overcoming several performance tradeoffs associated with SiC power MOSFET devices, while promising simple processing for the device fabrication.

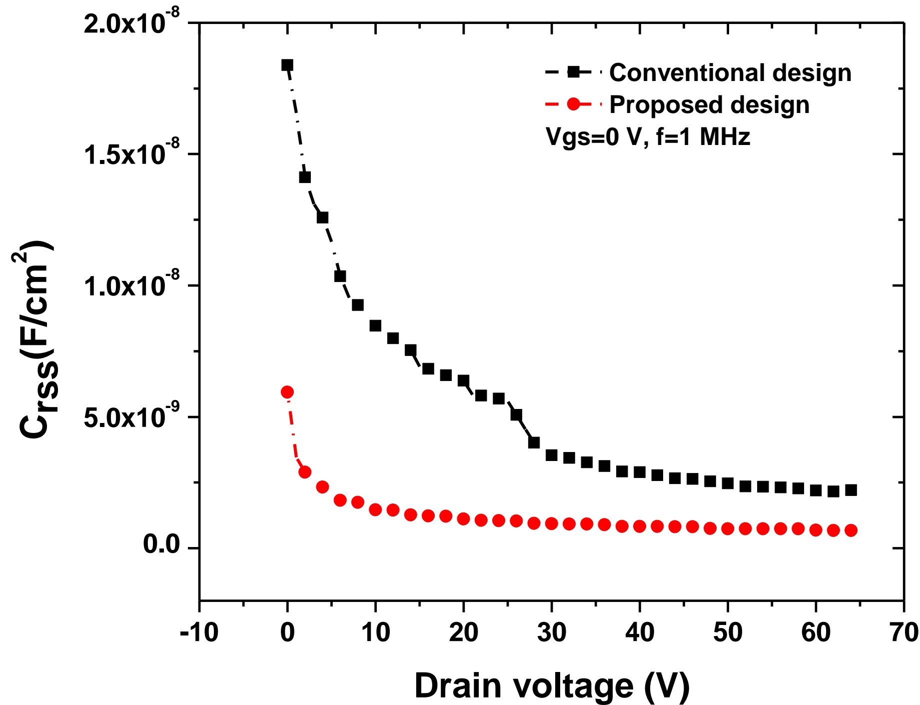
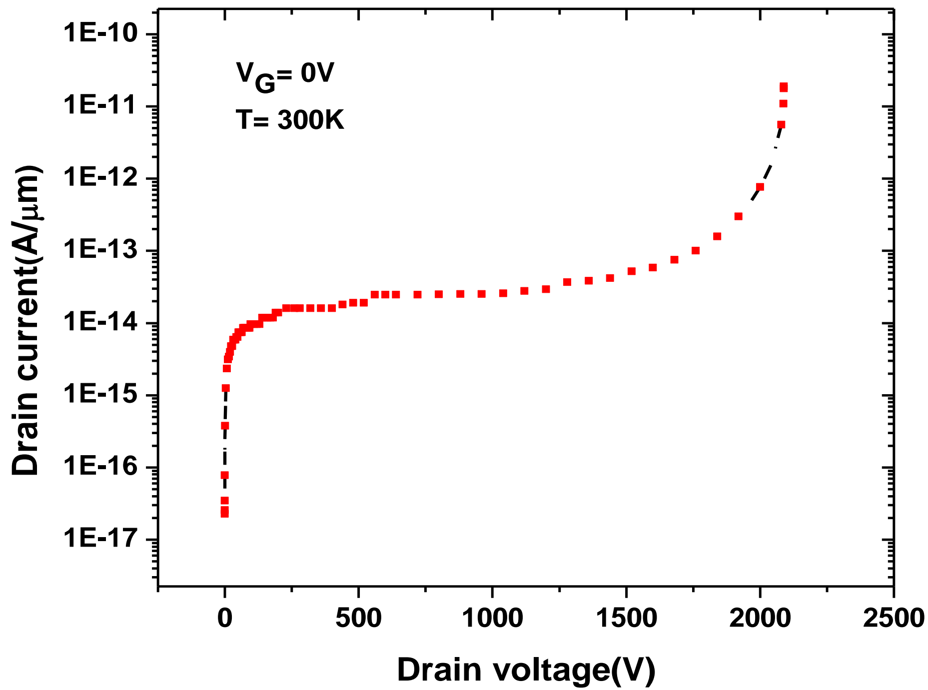


Figure 3.5 *Variation of reverse transfer capacitance against drain voltage for Vgs=0V and f=1MHz.*

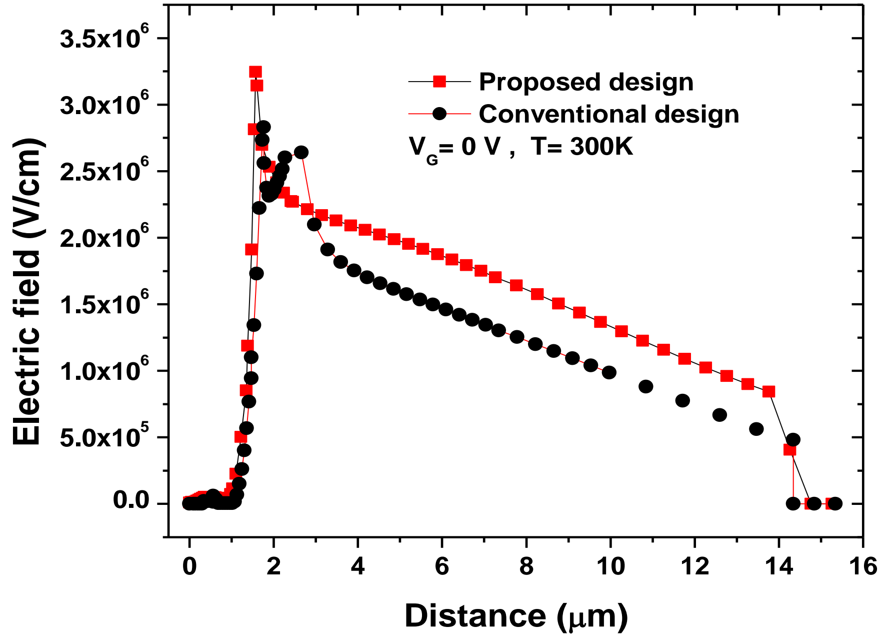
3.3.3 Breakdown simulation

To evaluate the breakdown characteristics of the proposed SiC power MOSFET based on combined gate trench engineering and JL technology, Fig.3.6 (a) depicts the variation of the drain current as a function of the drain voltage at blocking mode (V_{gs}=0 V) and at room temperature conditions. Observing this figure, we can notice that the breakdown region starts around 2 KV, indicating the superior breakdown characteristics of the proposed device with combined gate trench and JL aspects. To elucidate the main reasons behind this interesting breakdown characteristic, Fig.3.6 (b) shows the electric field profiles of the investigated devices with and without JL paradigm at breakdown condition across the specific path a-b-c as illustrated in Fig.3.1 (a). As shown in this figure, the proposed device with JL structure exhibits higher electric field

values over the b-c cutline, thus demonstrating its ability for supporting high critical electric field values. Fig.3.6 (c) shows the critical electric field contours associated with the proposed SiC trench power MOSFET with JL structure at breakdown. This profile shows that the breakdown region is located at the gate edge, proving a high value of 3.93 MV/cm. The latter value is higher than that provided by recently improved high-performance devices without JL paradigm [23]. Therefore, getting rid of metallurgical junctions using JL technology can provide new directions for overcoming the most pronounced challenges associated with SiC power MOSFET devices, offering low ON-resistance, high derived current, reduced power consumption, superior breakdown characteristics and enhanced switching properties.



(a)



(b)

(c)

Figure 3.6 *Breakdown characteristic of the proposed JL trench power MOSFET. (b) Electric field distribution at breakdown conditions across the cutline path of a-b-c for both the proposed JL power MOSFET. (c) The electric field profile at the breakdown region of the proposed JL power MOSFET.*

For the completeness of this work, a performance assessment of the proposed SiC power MOSFET device based on combined gate-trench engineering and JL technology is carried out by comparing its performances with other common strategies based on super junction, conventional gate-trench, double trench and planar structures [14], [23] and [28-29]. The obtained results are summarized in Table 3.2

Table 3.2 *Performance comparison of the proposed device with other devices with dissimilar structure engineering strategies.*

References	POWER MOSFETS	BV (V)	$R_{On,sp}$ ($m\Omega.cm^{-2}$)	FOM ($V^2/m\Omega.cm^{-2}$)	Elaboration Cost
[23]	DT-MOS	1554	2.07	1167	High
[23]	C-TMOS	1486	2.11	1046	High
[23]	SJ-TMOS	1633	1.14	2339	High
[28]	LSG-MOS	1230	6.39	236	High
[28]	DSS-MOS	1235	2.58	591	High
[29]	Device A	1500	2.4	938	High
[29]	Device B	1560	2.02	1203	High
[14]	Planar JL-MOS	2676	5.78	1236	Low
This work	JL-TMOS	2057	1.64	2580	Low

The latter table demonstrates that the proposed device can outperform greatly the conventional counterparts in terms of breakdown characteristics, energy loss and fabrication cost. Despite these outstanding results, super junction-based devices show lower ON resistance as compared to the proposed device with JL and oxide trench aspects. This is quite logical because of the use of oxide trench regions, leading to slightly enlarge of the ON resistance. However, the proposed device exhibits less processing complexity and low power dissipation as compared to the structures based on super junction strategy. These enhancements in terms of energy loss, switching speed and breakdown properties confirm the beneficial role of using combined JL and gate-trench strategies for the development of cost-effective, high-performance SiC Power MOSFETs. It is important to note that the geometry parameters of the introduced oxide trench regions can be optimized to boost up the device performances using metaheuristic-based optimization approaches.

However, new complex calculation models based on combining 2D numerical device simulations and metaheuristic-based computations should be developed [30-32].

3.4 Conclusion

In this chapter, a novel SiC power MOSFET device based on combined gate-trench and JL strategies is proposed and investigated by developing accurate numerical models. The main idea behind the proposed device dwells on introduced symmetrical oxide regions based on grooves-like shape to develop a JL structure. The impact of the oxide geometry on the device characteristics is also investigated. It is demonstrated that the proposed device shows reduced threshold voltage due to the use of JL structure, promoting low power consumption characteristics. It is found that the proposed SiC trench power MOSFET with JL aspect exhibits low energy loss and superior switching speed as compared to the conventional one, offering reduced ON-resistance of 1.6 $m\Omega/cm^2$ and lower HF-FoM of 1078 mΩ.pF. In addition, it demonstrates superior breakdown properties with a high BV exceeding 2 kV and a high FoM of 2580 $V^2/m\Omega.cm^{-2}$. This outstanding result is attributed to its ability to support high critical electric field near the gate edge of 3.93 MV/cm. Therefore, we believe that the presented investigation can provide new guidelines for the design of high-performance cost-effective SiC power MOSFET, which can be potential alternative for the emerging electronic power systems.

3.5 References

[1] Z. Tong, L. Gu, Z. Ye, K. Surakitbovorn, J. Rivas-Davila, "On the techniques to utilize SiC power devices in high- and very high-frequency power converters", IEEE Trans. Power Electron, vol. 34, pp. 12181–12192, 2019.

[2] S. Dimitrijev, "SiC power MOSFETs: the current status and the potential for future development", in: 30th IEEE International Conference On Microelectronics (MIEL), Nis, Serbia, Oct 2017, pp. 29–34, 2017.

[3] Rakesh Vaid et al, "A novel trench gate floating islands power MOSFET (TG-FLIMOSFET): Two-dimensional simulation study," Microelectronic Engineering, 88, 11, pp. 3316–3326, 2011.

[4] H. Fu et al. "1200V 4H-SiC trench MOSFET with superior figure of merit and suppressed quasi-saturation effect," Microelectronics Reliability, vol. 123, pp. 114249, 2021.

[5] J. L. Afonso et al, "A Review on Power Electronics Technologies for Power Quality Improvement," Energies, vol. 14, pp. 8585, 2021.

[6] P. Vudumula, S. Kotamraju, "Design and optimization of SiC super-junction MOSFET using vertical variation doping profile," IEEE Trans. Electron. Dev, vol. 66, pp. 1402–1408, 2019.

[7] W. Cao et al, "A novel SiC superjunction MOSFET with three-level buffer and unipolar channel diode," Micro and Nanostructures, vol. 172, pp. 207420, 2022.

[8] P. Nautiyal, A. Naugarhiya and S. Verma, "An Assessment of Step Patterned Gate Oxide Superjunction Trench MOSFET for Potential Benefits," Journal of Electronic Materials, vol. 48, pp. 8156–8162, 2019.

[9] E. O. Prado, P. C. Bolsi, H. C. Sartori and J. R. Pinheiro, "An Overview about Si, Superjunction, SiC and GaN Power MOSFET Technologies in Power Electronics Applications," Energies, vol. 15, pp. 5244, 2022.

[10] D. V. Mauricio, et al. "Gallium-nitride semiconductor technology and its practical design challenges in power electronics applications: An overview," Energies, vol. 12, pp. 2663, 2019.

[11] M. Cédric, N. Rouger, J. Pernot, "Recent progress in deep-depletion diamond metal–oxide–semiconductor field-effect transistors," Journal of Physics D: Applied Physics, vol. 54, pp. 233002, 2021.

[12] V. Pavan Kumar Reddy et al, "Improved device characteristics obtained in 4H-SiC MOSFET using high-k dielectric stack with ultrathin SiO_2-AlN as interfacial layers," Materials Science in Semiconductor Processing, vol. 80, pp. 24–30, 2018.

[13] Z. Bai et al, "Improving avalanche robustness of SiC MOSFETs by optimizing three-region P-well doping profile," Microelectronics Reliability, vol. 124, pp. 114332, 2021.

[14] B. Zerroumda, F. Djeffal, S. Benaggoune, H. Ferhati, "Performance assessment of a novel 4H–SiC junctionless planar power MOSFET towards improving electrical properties," Micro and Nanostructures, vol. 169, pp. 207346, 2022.

[15] J.P Colinge, C.W. Lee, A. Afzalian, et al, "Nanowire transistors without junctions," Nat Nanotechnol, vol.53, pp. 225–229, 2010.

[16] H. Ferhati and F. Djeffal, "Graded channel doping junctionless MOSFET: a potential high performance and low power leakage device for nanoelectronic applications," Journal of Computational Electronics, vol. 17, pp. 129-137, 2018.

[17] H. Ferhati and F. Djeffal, "Planar junctionless phototransistor: A potential high-performance and low-cost device for optical-communications," Optics & Laser Technology, vol.97, pp.29-35, 2017.

[18] B. Zerroumda, F. Djeffal, S. Benaggoune, H. Ferhati, "Investigation of a new power junctionless MOSFET using 2-D numerical simulation," IEEE 19th International Multi-Conference on Systems, Signals & Devices (SSD), 2022.

[19] S.M. Abd El-Azeem, S.M. El-Ghanam, "Comparative study of gallium nitride and silicon carbide MOSFETs as power switching applications under cryogenic conditions," Cryogenics, vol. 107, pp. 103071, 2020.

[20] ATLAS user manual: Device simulation software, 2012.

[21] M. J. Marinella et al, "Carrier Generation Lifetimes in 4H-SiC MOS Capacitors," IEEE Trans, Electron Devices, vol. 57, pp. 1910-1923, 2010,

[22] T. Hatakeyama et al, "Impact ionization coefficients of silicon carbide," Appl. Phys. Lett., vol. 85, pp.1380, 2004. doi: 10.1063/1.1784520.

[23] Q. He, X. Luo, T. Liao, J. Wei, G. Deng, T. Sun, J. Fang, F. Yang, "4H-SiC superjunction trench MOSFET with reduced saturation current," Superlattices and Microstructures, vol. 125, pp. 58-65, 2019.

[24] Y. Zhang, S. Bai, R. Huang, T. Zhang, "4H–SiC trench MOSFET with Inverted-T groove," Micro and Nanostructures, vol. 175, pp. 207510, 2023.

[25] Y. Zhou, Z. Wang, G. Xin, J. Yuan and X. Shi, "Dead Time Optimization for Synchronous Switching of SiC MOSFETs Considering Nonlinear Gate Capacitance," IEEE Transactions on Power Electronics, 2023.

[26] G. L. Rødal, Y. V. Pushpalatha, D. A. Philipps and D. Peftitsis, "Capacitance Variations and Gate Voltage Hysteresis Effects on the Turn-On Switching Transients Modelling of High-Voltage SiC MOSFETs," IEEE Transactions on Power Electronics, 2023.

[27] Y. Cai et al., "Effect of Threshold Voltage Hysteresis on Switching Characteristics of Silicon Carbide MOSFETs," IEEE Transactions on Electron Devices, vol. 68, pp. 5014-5021, 2021.

[28] G. Liu et al, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," Journal of applied physics, vol. 2, pp. 021307, 2015.

[29] S. Hu et al. "A low specific on-resistance power trench MOSFET with a buried-interface-drain," Superlattices and Microstructures, vol. 85, pp. 133–138, 2015.

[30] H. Ferhati, F. Djeffal, L.B. Drissi, "Metaheuristic-based decision maker framework for the development of multispectral IGZO thin-film phototransistors," Journal of Science: Advanced Materials and Devices, Vol. 7, pp. 100414, 2022.

[31] H. Ferhati, F. Djeffal, "A novel high-performance self-powered ultraviolet photodetector: Concept, analytical modeling and analysis," Superlattices and Microstructures, vol. 112, pp.480-492, 2017.

[32] T. Bendib, F. Djeffal, "Electrical Performance Optimization of Nanoscale Double-Gate MOSFETs Using Multi-objective Genetic Algorithms," IEEE Trans on Electron Devices, Vol. 58, pp. 3743 – 3750, 2011.

Chapter 4

4H-SiC MOSFET design using high-k materials and circuit level analysis of the impact of our proposed device on power electronics applications.

Abstract- *In this chapter, a numerical analysis using TCAD-based computation provided by ATLAS 2D simulator is carried out. The first part of this chapter presents a comprehensive investigation of the impact of various high-k gate materials on both breakdown voltage and drain current of a vertical 4H-SiC-based power MOSFET, operating in the quasi-saturation regime. The effect of the dielectric permittivity on the derived current capability is also analyzed. After, we conduct a sensitivity analysis of the breakdown voltage with several high-k materials (Al2O3, HfSiO4, HfO2, and TiO2) and different dielectric thicknesses. The second part aimed at analyzing the performances of the effect of combining the Junctionless technology and the gate-trench strategy for improving the electrical and switching performances of SiC power MOSFETs. A circuit level analysis using Atlas mixed mode module is performed in order to assess our proposed device performances for power electronic applications. More specifically, the device switching performances are analyzed in a circuitry related to a resistive load, then related to an inductive load. In the first part, It is found that the proposed high-k use in SiC-MOSFET design exhibits an improved electrical behavior, enabling not only to enhance the drain current but also allows achieving superior breakdown performance as compared to the conventional design, making it suitable for high-performance power electronic applications. As for the second part, it is found that the strategic combination between both JL and gate-trench aspect can enable achieving enhanced electrical, and switching performances in power conversion circuits. Therefore, we believe that the proposed device can be suitable for the development of efficient and low-cost DC-DC power converters for photovoltaic MPPT.*

Part .1: The use of high-k materials in the design of 4H-SiC MOSFET to improve the quasi-saturation regime

4.1.1 Introduction

Power devices are a mandatory requirement for applications operating over a broad spectrum of power levels. Among these applications, we have a category that necessitates high operating voltages (above 200V) [1]. For this reason, high-k materials should meet several characteristics to be deployed in power metal oxide semiconductor field effect transistors (Power MOSFET) applications namely: a large dielectric constant, a large band-gap energy, a thermal stability, a large effective mass for tunneling carriers, a good integrity of high-k/substrate interface, and a high reliability against electrical stresses [2]. Recently, several research projects are elaborated on metal oxide materials with high-k values which have the ability to be integrated in MOSFET, and many researchers are focused on high-k materials used with semiconductors to improve the device substrate [3-5].There are many high-K dielectrics that are being studied currently such as HfO_2, TiO_2, and Al_2O_3 [6]. The unipolar power MOSFET integrates a high voltage drift region in its structure (Figure-1). The breakdown voltage of a power MOSFET is determined by the doping level of the drift epitaxial layer and its thickness [1]. Unlike the standard MOSFET, in power MOSFET devices we observe, at high gate and drain voltages, a decrease of drain current level as shown in (Figure-2). [7] It is recognized that there exist two mechanisms which restrict the drain current and lead the MOSFET into quasisaturation. These are: the high resistivity of the drift region, and the formation of a gate independent dipole layer [8]. The quasisaturation effect arises in several power MOSFET structures like conventional, trench and super-junction power MOSFET devices [9]. Therefore, the quasi-saturation effect must gain more attention during the study of power MOSFET devices. For the high saturated electron drift velocity, large band-gap, elevated thermal conductivity, and high breakdown voltage, SiC alloy is considered as the appropriated material to fabricate the high power, high temperature, compact, and high frequency devices [10]. Having realized the importance of the study of 4H-SiC power MOSFET operating in quasi-saturation regime, and containing high-k materials, we have started our work using ATLAS-2D simulator to highlight the impact of high-k materials. Such impact is accentuated on both the drain current quasi-saturated due to the carrier velocity saturation in the drift region, and on the behavior of the breakdown voltage, to increase its value without changing the doping level or the

drift region thickness. So, we do not need in this case to increase the Ron resistance of the drift region. The remaining of this paper is arranged as follows. In section 2, we present the numerical modeling of the device with the principal simulation parameters. In section 3, we show the main obtained simulation results. Finally, some concluding remarks are provided.

4.1.2 Numerical simulation

With the current development of computer-aided design tools, the behavior description of complex physical systems becomes more flexible and tends to replace the carry of complicated physical experimentation. In this section, we focus on the illustration of our numerical simulation framework including the considered physical phenomena models.

4.1.2.1 Device Design

Figure 4.1 presents the structure of the conventional power VMOSFET used as a prototype for comparison purposes. This MOSFET has a symmetrical structure where both the source/drain N+ regions are heavily doped. These two regions are characterized by high doping values in comparison to the substrate denoted by P. Two heavily doped regions denoted by P+ are inserted between the source electrodes and the p-substrate in order to suppress the parasitic PNP bipolar transistor. The drift region of this MOSFET is composed of two parts; the first is delimited by the two P-Substrate regions, where a JFET structure in this case can be distinguished. Whereas, the second is located between this layer and the N+-substrate layer. Despite that this region has the specificity of being lightly doped; its upper layer is slightly more doped than the lower layer for reasons of optimization. This will results in an improvement of the iron-resistance.
The minimum channel length is restricted by the reach through phenomenon in addition to the value of the blocking voltage, because the depletion width in the P-base layer increases when the N drift layer doping concentration is decreased [1]. The gate electrode is made of n polysilicon, while the gate dielectric is composed of an oxide layer with a thickness of 5 nm, and a high-k layer of the same thickness. This configuration is adopted during the behavior simulation of the drain current and the breakdown voltage when varying high-k materials. The geometrical and electrical parameters related to this power MOSFET are illustrated in Table 4.1

Table 4.1 *Simulation parameter values of the conventional vertical power MOSFET structure.*

Symbol	Power VMOSFET
Channel length L(nm)	**1500**
Oxide layer thickness (nm)	**5**
High k layer thickness (nm)	**5**
N+ S/D doping concentration (cm^{-3})	**$1x10^{20}$**
P-base doping concentration (cm-3)	**$1x10^{17}$**
P-base depth (nm)	**2400**
Gate work function (eV)	**1.37**

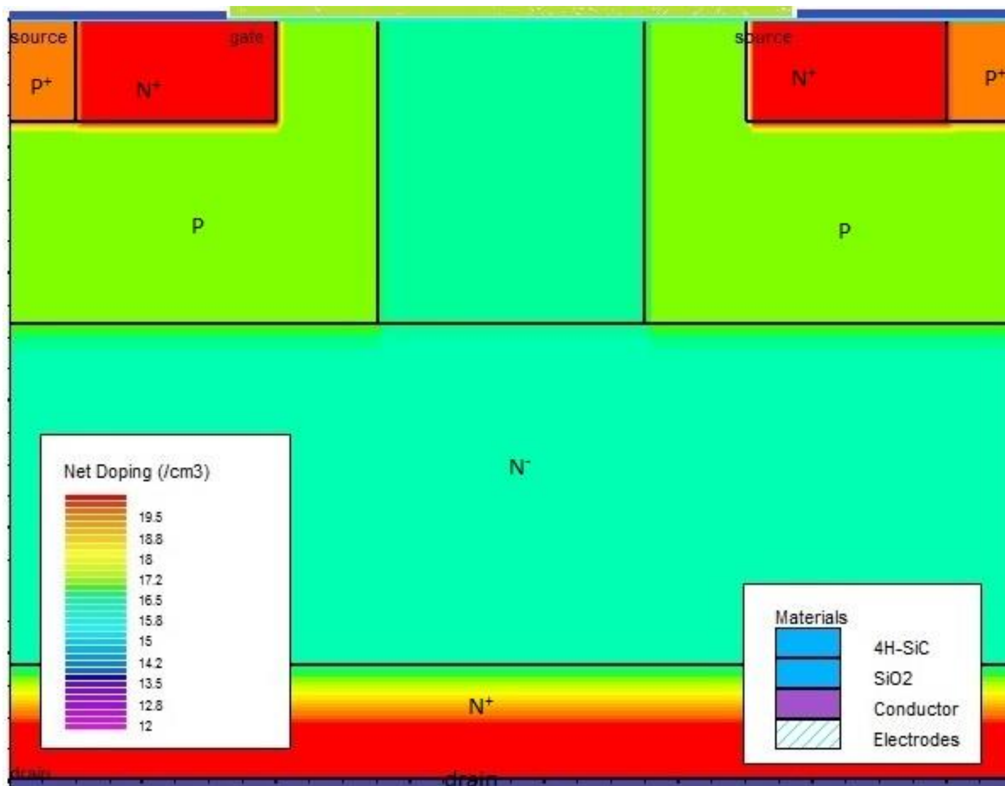


Figure 4.1 *Cross-sectional view of the conventional vertical power MOSFET considered in this study.*

The formula, which relates the equivalent dielectric permittivity to the permittivities of the oxide and the high-k material, is expressed by [11]:

$$\varepsilon_{eq} = (\varepsilon_1\varepsilon_2)(t_1 + t_2)/(\varepsilon_2 t_1 + \varepsilon_1 t_2) \qquad (4.1)$$

4.1.2.2 Simulation models

This subsection presents the models implemented into the commercial ATLAS simulator that have been considered in the simulation. First, it is important to know that when we carry out a simulation work, a number of severe constraints is imposed. Such situation does not only determine the complexity of the problem, but also reveals the intrinsic nature of the system. Therefore, the most accurate simulation framework requires being as close as possible to the nature of the system, where various physical phenomena should be accounted. The model of Shockley, Read, and Hall, known as SRH model, gives the statistics for the recombination of electrons and holes in semiconductors, it was first treated independently by Shockley and Read, then by Hall. Their analysis shows the rate of recombination in the steady state through a single deep level recombination center [1]. This model is widely used to describe the impact of deep impurities on device characteristics [12]. The Caughey-Thomas formula. Tuned for 77-450K., denoted ANALYTIC, is an analytic low field mobility model that is used to relate the low field carrier mobility to impurity concentration and temperature [13]. The Auger phenomenon, denoted "auger", is a physical process of carrier recombination in which, the energy released during the recombination process is transferred not to a light quanta but to a third particle, where a participation of a phonon can be necessitated for conservation of momentum. [9]. The underlying physics for such process is unclear and consequently more rigorous studies are needed [14]. When the electric field becomes high, the average mobility becomes inversely proportional to the electric field magnitude. This implicates that the velocity for the free carriers becomes constant at a given value; this phenomenon is referred to as drift velocity saturation [1]. Its model in ATLAS is denoted "fldmob". The Lombardi mobility model, denoted "cvt", is based upon three components of the mobility, The first component, is the surface mobility limited by scattering with acoustic phonons, The second component, is the mobility limited by surface roughness, The third mobility component, is the mobility limited by scattering with optical phonons[15].

4.1.3 Results and discussion

In Figure 4.2, we show the simulated transfer characteristics obtained with the studied power VMOSFET for different gate voltages. In this figure, it is clearly observed that the quasi-saturation regime starts for a specific gate voltage value of V_{gs} = 7 V. When this phenomenon takes effect, the drain current equals to 18.7 A for V_{gs} = 7 V and V_{ds}=30V. Afterward, by increasing V_{gs} to 8V, the current reaches 19.2 A, where the increase in the derived current capability of the investigated design is about 0.5 A only. Whereas in normal regime, the drain current for V_{gs}=5V and V_{ds}=30 V is equal to 9.1 A. It should be mentioned that when the gate voltage equals to 6V, the current reaches 14.9A and the difference in this case is very large. We can observe also that when V_{gs} is higher than 7V, the drain current becomes insensitive to further changes of V_{gs}. Thus, the quasi-saturation effect could limit the current support capability of the device.

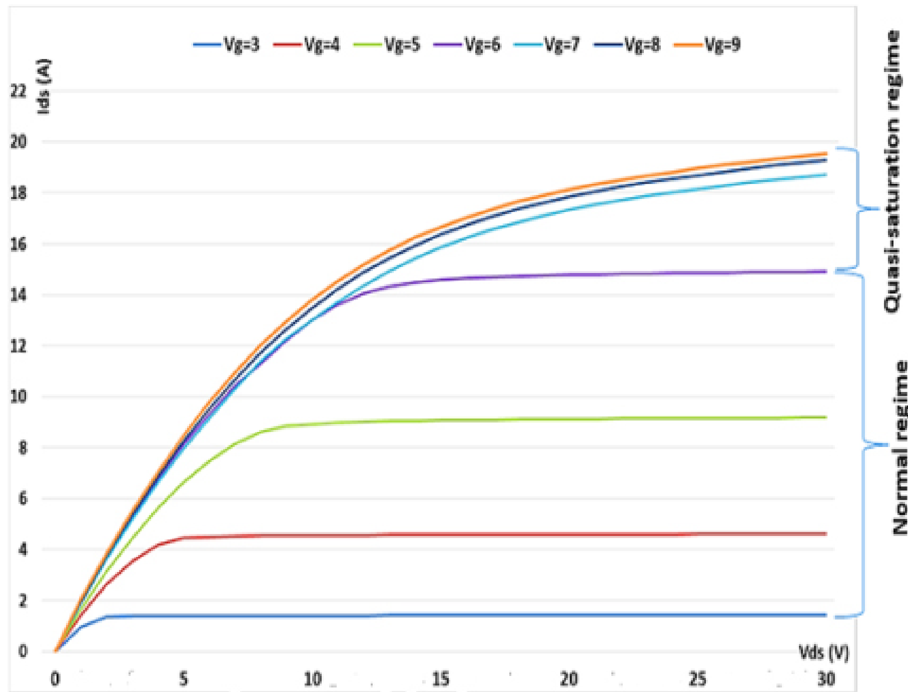


***Figure 4.2** Output characteristic of the studied conventional power VMOSFET*

Aiming at elucidating the impact of oxide dielectric permittivity on the device performance, Figure 4.3 shows the variation of the drain current versus different high-k dielectric materials with V_{gs} = 7 V and V_{ds} = 30. It can be obviously observed from this figure that by increasing the material dielectric permittivity, the drain current is increased. Moreover, in comparison with the drain current associated to SiO2 having a value of 18.7A, we notice an enhancement with the increase

of the permittivity. This can be attributed to the enhanced control of the channel electrical behavior offered by the introduced high-k material. In other words, the insertion of high-k materials can provide the possibility for effectively controlling the channel conductivity behavior.

Table 4.2 summarizes the simulation values of the derived current for different gate dielectric materials. This table confirms the effectiveness of the introduced high-k material for enhancing the drain current as compared to the conventional design.

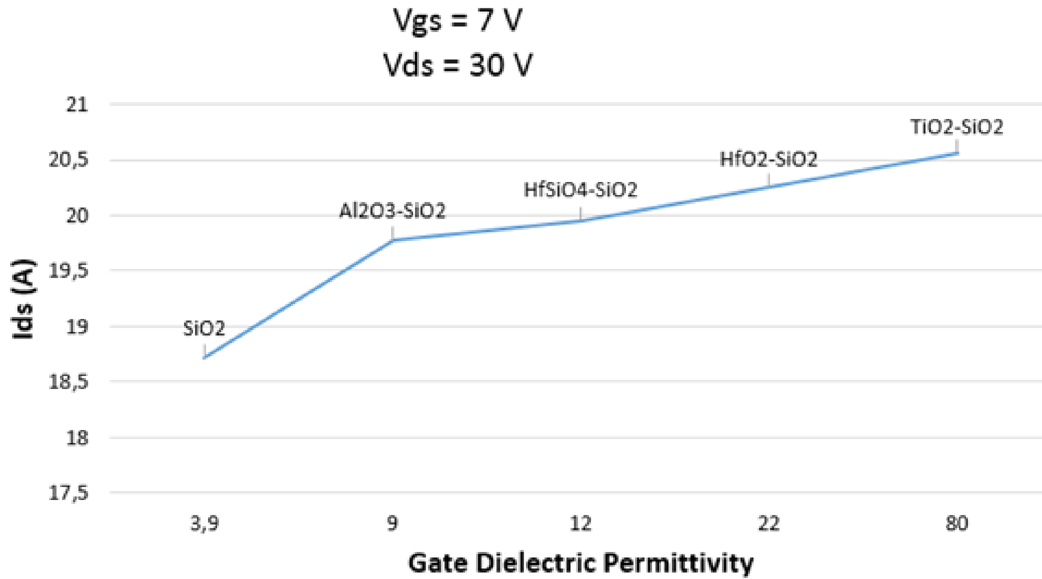


Figure 4.3 *Variation of the drain current in quasi-saturation regime with respect to gate dielectric permittivity using different high-k materials*

Table 4.2 *Simulation values of the drain current, with the increase associated to each gate dielectric*

Gate dielectric	Drain current	Increase Value (A)
Al_2O_3-SiO_2	**19.77**	**1.07**
$HfSiO_4$-SiO_2	**19.95**	**1.25**
HfO_2-SiO_2	**20.25**	**5**
TiO_2-SiO_2	**20.56**	**$1x10^{20}$**

Thus, by the use of high-k materials, we can consider that the operating point Vgs = 7 V belongs to the normal regime, and more improvements can be obtained with greater dielectric permittivities. However, we note that the increasing rate of the drain current is not linear.

The breakdown voltage is considered as important parameters for perfectly evaluating the investigated structure for power electronics application. To this extent, Figure 4.4 illustrates the variation of the breakdown voltage as a function of the gate dielectric permittivity. This figure indicates that the breakdown voltage in the quasi- saturation regime increases significantly with the increase of the dielectric permittivity value. Moreover, the breakdown voltage is shifted upper with a value of 60 Volts for Al2O3-SiO2, which can be seen as an acceptable amelioration. Besides, an increase of 87 V is observed for HfSiO4-SiO2. Whereas the breakdown voltage increases with an amount of 106 V for HfO2-SiO2 and 120 V for TiO2-SiO2. But we note, as like for the drain current, that the increasing rate of the breakdown voltage is not linear. On the other hand, the thickness of the gate dielectric material plays a crucial role in determining the power VMOSFET performance. In this framework, Figure 4.5 depicts the variation of the breakdown voltage as a function of the gate dielectric thickness for different high-k materials. The variation is applied to the high-k material thickness, where the oxide thickness is fixed at 5 nm.

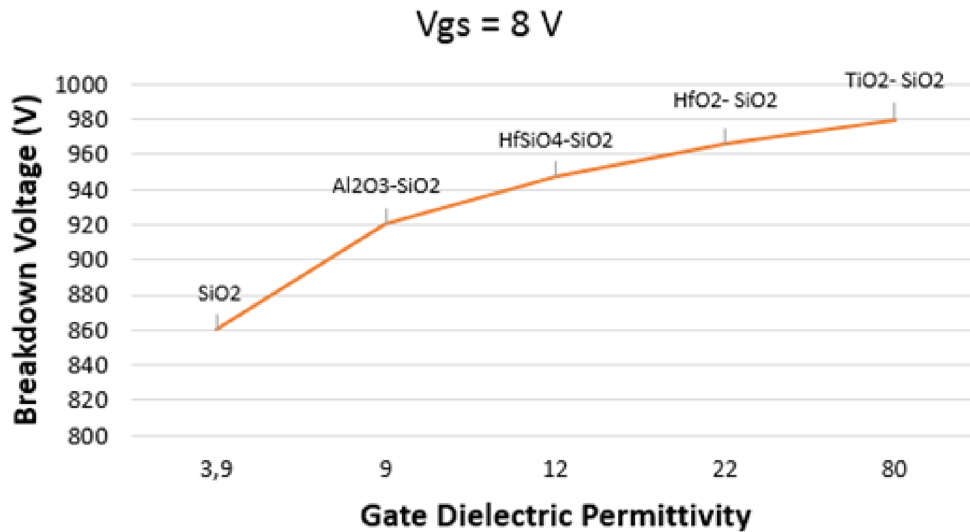


Figure 4.4 *Variation of the breakdown voltage in the quasi-saturation regime with respect to gate dielectric permittivity using different high-k materials.*

From Figure 4.5, we note that the breakdown voltage decreases with the increase of the gate dielectric thickness. We observe also that when the gate dielectric permittivity increases, the breakdown voltage is less sensitive to the increase of the gate dielectric thickness, it has a trend to be constant with respect to the increase of the gate dielectric thickness up till a certain value. This indicates the complex behavior associated with the proposed design with high-k materials, where

identifying the better combination of the high-k material as well as taking the elaboration cost into consideration seems interesting for achieving high-performance power VMOSFET device. For this purpose, metaheuristic techniques have been used to select the better design that provides enhanced performances of different micro and nano-electronic devices. As a matter of fact, these techniques have proven their appropriateness for optimizing different microelectronic devices [16-19]. Therefore, these techniques can be applied to boost up the performance of the investigated design and achieve higher values for both the drain current and the breakdown voltage.

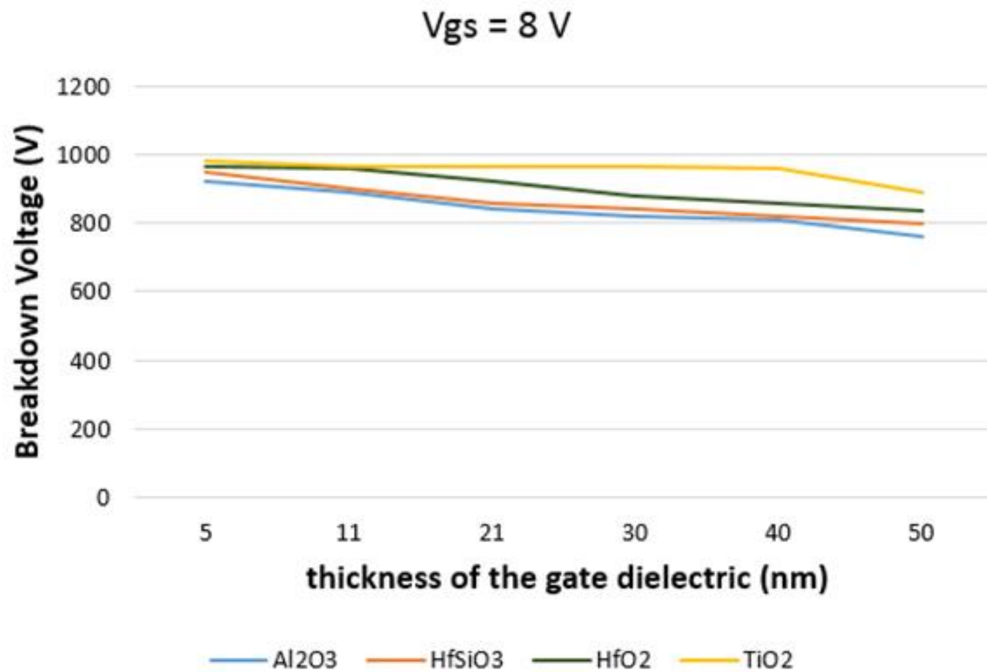


Figure 4.5 *Variation of the breakdown voltage in the quasi-saturation regime with respect to gate dielectric thickness for different high-k materials*

Part .2: The junctionless Power MOSFET for Photovoltaic Applications

4.2.1 Introduction

Power transistors based SiC building blocks are highly suitable for the development of effective power electronic circuits. The improvements related to the role of power MOSFETs in photovoltaic systems is to reduce switching losses and to increase switching frequency [20-24]. In that perspective, we have demonstrated in the past chapter that the proposed power MOSFET exhibits low switching losses and high switching frequency compared to the conventional case owing to its high switching figure of merit backed by its low input and transfer capacitances.

Therefore, the device begins to switch-on at very low applied gate voltages, demonstrating its ability for offering suitable commutation characteristics with ultralow power consumption.

In the previous work, we have addressed the performance issue far from the circuit aspect, i.e. we have shown the inherent performances of the discreet device alone, not its performances delivered when the device is arranged in an electrical circuit [25]. Thereby, in this part we intend to demonstrate the effectiveness of our proposed power MOSFET in terms of commutation speed in an electrical assembly, in which the load is considered differently in two examples, one of a resistive load, and the other of an inductive load.

4.2.2 Commutation speed in the case of a resistive load

To analyze the transistor commutation characteristics, the JL device with gate trench is used for the design of a resistive load circuit as it is depicted in Fig 4.6. In this context, mixed mode module is exploited to perform to a circuit level analysis, where the load resistance is fixed at 10 kΩ, and the gate input voltage is taken to be a pulse signal in a trapezoidal form with a rise time of 10 ns. The input signal is applied in the first case with one alternation, to show the rise time of the junctionless power MOSFET compared to its conventional counterpart as illustrated in Fig 4.7. Then, an input signal with tow alternations and a frequency of 10 MHz is applied to the gate, in order to highlight the high switching frequency of the JL structure alongside the improved rise time as shown in Fig 4.8.

Actually, a very impactful result can be taken from figure 4.7 showing the drain voltage as a function of the transient time, in which the input signal is applied to control the JL MOSFET gate. This important outcome, to begin with, is that the JL structure response is characterized by a rise time from 0.5 V to 38.5 V of 38 ns compared to a rise time of 56 ns for the conventional counterpart in the same voltage range. It is worth mentioning that the rise time of the JL structure 1ns/V is equal to the rise time of the input signal. Whereas, the rise time of the conventional counterpart is 1.49 ns/V. With respect to the delay time, we notice comparable values for both structures around 14 ns.

In figure 4.8, the input signal frequency is increased to 10 MHz, and the numerical simulation is performed for two periods. The results prove the suitable switching characteristics of the suggested transistor based on combining JL aspect and gate-trench aspect as the proposed device output is less affected by the elevation of the frequency, which means that it can reach frequencies that are higher than its conventional counterpart. Furthermore, a reduced rise-to-fall time, which is the time

spent between a rise from and a descent to the off state, can be seen in figure 4.8. Where, clearly, the proposed structure spends a smaller time to reach higher values and then returns to the off state, which is represented by the fact that while reaching higher values the JL curve is contained along the time axis within the conventional counterpart curve.

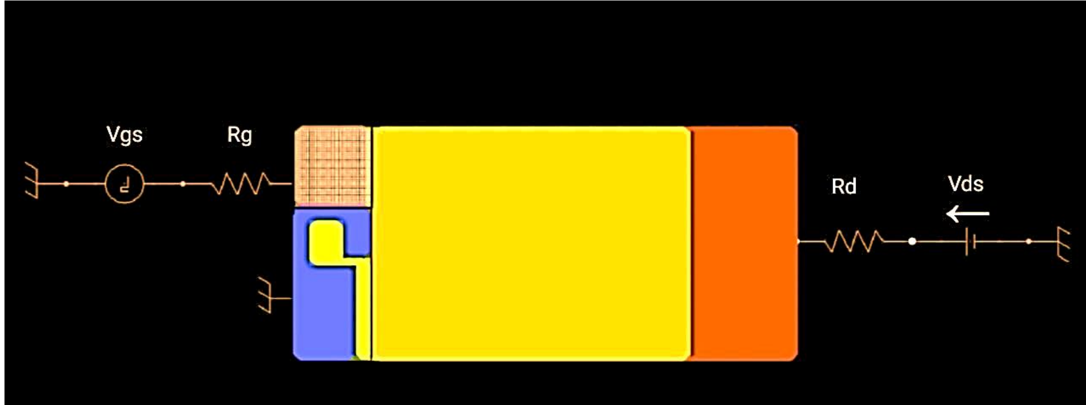


Figure 4.6 *Mixed mode simulation schematic of the junctionless trench power MOSFET in the case of an inductive load*

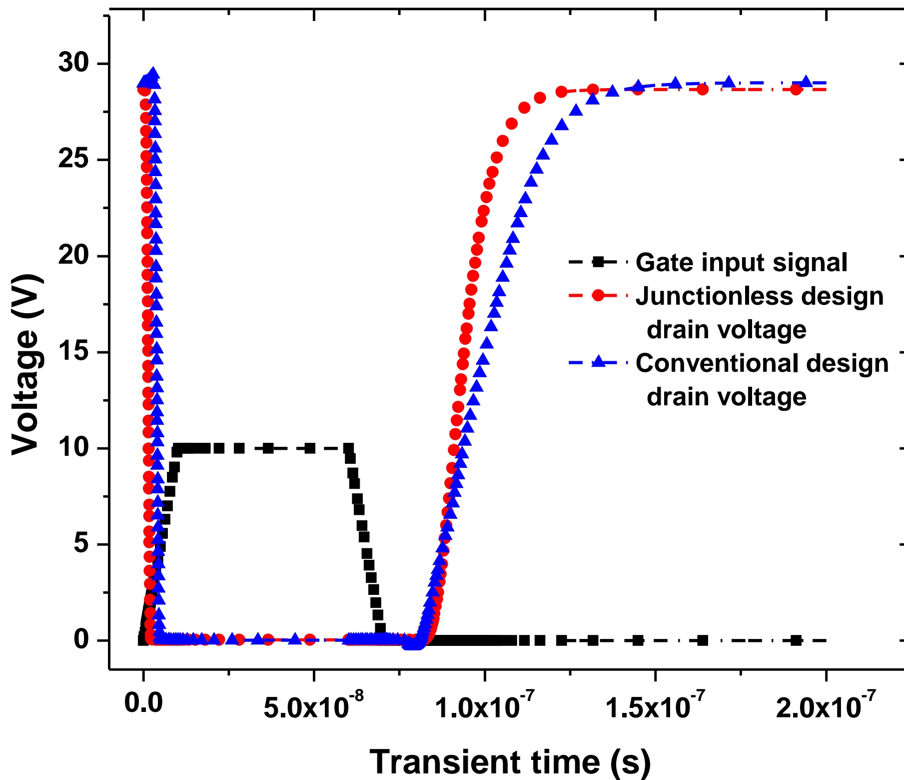


Figure 4.7 *plot of the drain voltages of both the junctionless trench power MOSFET and its conventional counterpart as functions of the transient time in the resistive load case and one alternation of the 8 MHz input signal.*

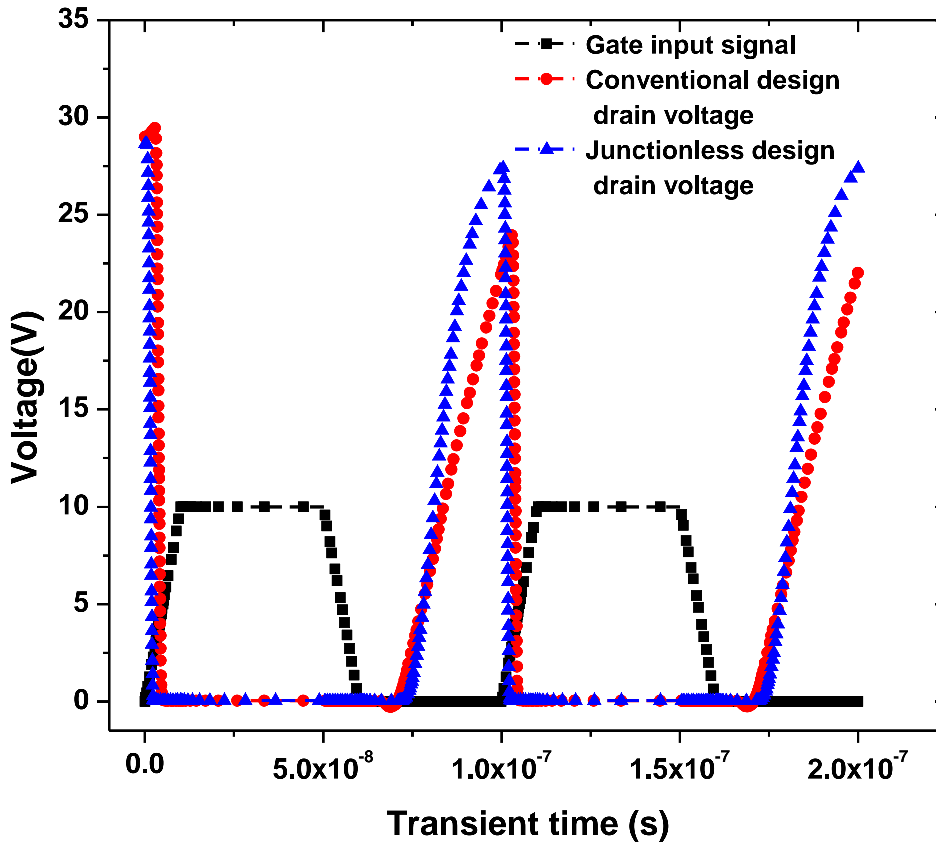


Figure 4.8 *plot of the drain voltages of both the junctionless trench power MOSFET and its conventional counterpart as functions of the transient time in the resistive load case and two alternations of the 10 MHz input signal*

4.2.3 Commutation speed in the case of an inductive load

In this subsection a circuit level investigation similar to that of the previous subsection is carried out, where both the investigated gate-trench JL SiC power MOSFET and its conventional counterpart are considered each one for the design of an inductive load circuit to assess their switching capabilities, and compare their performances. The inductive load is fixed at 5 mH, and the input signal applied to the gate electrode is a periodic pulse signal of a trapezoidal form with a rise time of 10 ns.

Figure 4.10, represents the drain voltage of both structures as a function of the transient time with a gate input signal of 8 MHz frequency applied for four alternations. From this figure, we can notice that in one hand, the rise time in the junctionless case is higher than that of its conventional counterpart, and in the other hand, the difference in rise time between the two structures is much more pronounced in the inductive load case than in the resistive load case. Furthermore, we observe that the rise time difference increases, as the maximum value reached in each alternation

is lesser than half the absolute maximum reached in all alternations. After surpassing half the absolute maximum in the subsequent alternations, the difference decreases as the rise time of the junctionless structure itself is nearing its maximum value. The rise time in each alternation is summarized in table 4.3

Table 4.3 *rise time values of both the proposed junctionless trench power MOSFET and its conventional counterpart in each alternation*

alternations	**1**	**2**	**3**	**4**
Conventional structure rise time (ns/V)	6	2.17	0.91	0.57
Junctionless structure rise time (ns/V)	2.64	0.75	0.46	0.46

In figure 4.11, the frequency of the gate input signal is reduced to 4 MHz. In fact, the contribution of this figure is the clarification of a misconception insinuated by figure 4.10. This figure may give a perception that the conventional structure is provided with an advantage over the proposed junctionless structure, which is the dissipation of the inductive power through the body diode when the device is in the blocking state, contributing, as such, to the device ruggedness. However, figure 4.11 gives us more clarifications, in which both structures have the same dissipation capability, and the proposed structure is provided with a comparable mechanism, which is to be identified in further studies. In that sense, the drain voltage of each structure reaches the same maximum value, but in different durations, and this difference can be regarded as a delay time. Indeed, the fact that the drain voltage of the conventional structure reaches the absolute maximum in the second alternation as the frequency is decreased, consolidates this explanation, which means that it is a matter of slow response not a matter of high performance in dissipating power.

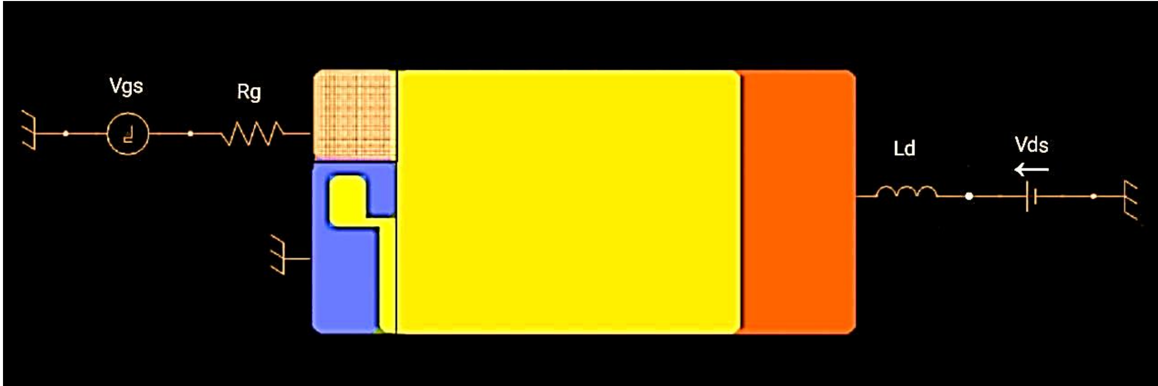


Figure 4.9 *Mixed mode simulation schematic of the junctionless trench power MOSFET in the case of an inductive load*

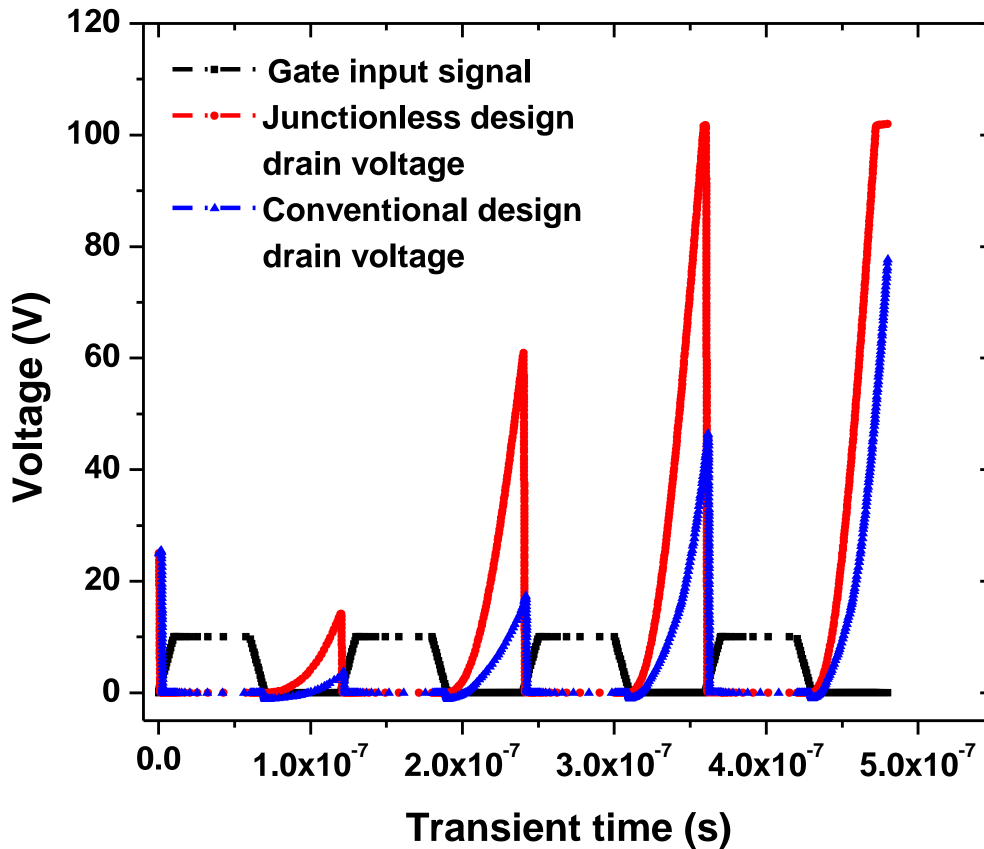


Figure 4.10 *plot of the drain voltages of both the junctionless trench power MOSFET and its conventional counterpart as functions of the transient time in the inductive load case and four alternations of the 8 MHz input signal*

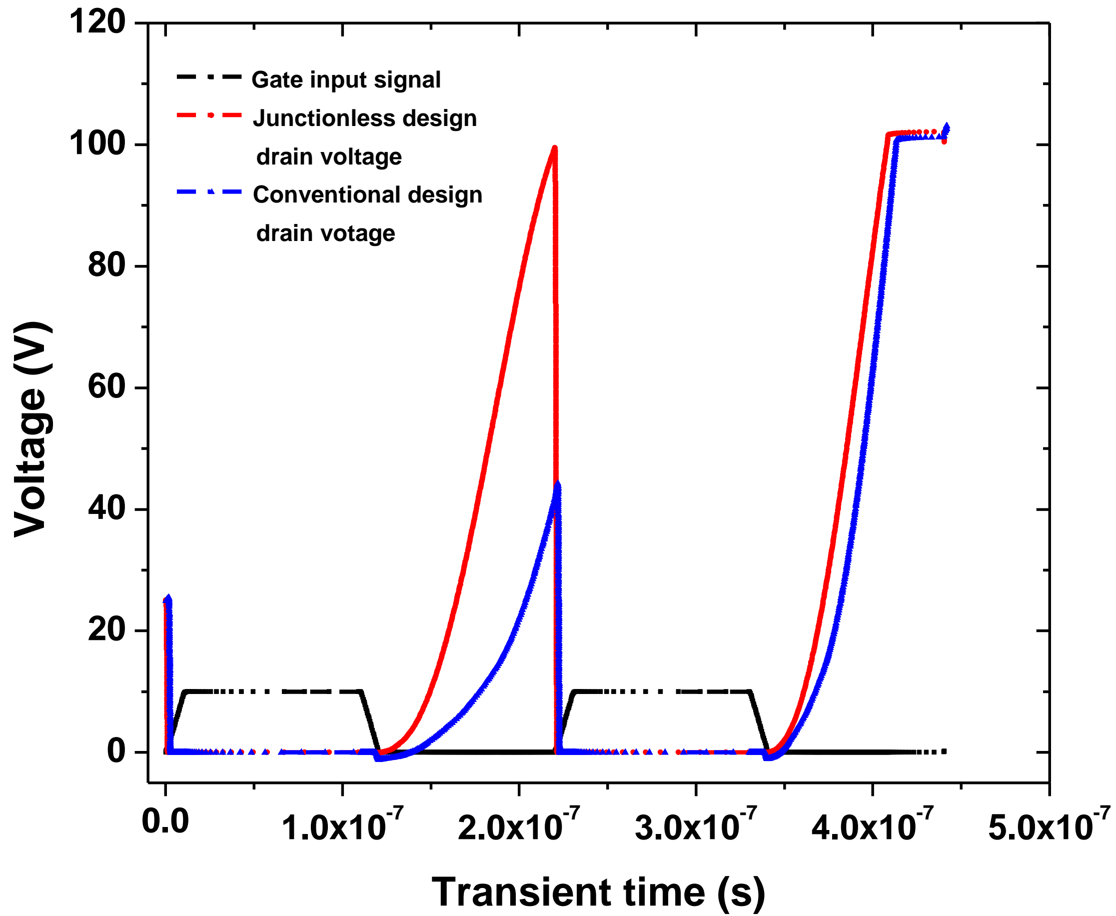


Figure 4.11 *plot of the drain voltages of both the junctionless trench power MOSFET and its conventional counterpart as functions of the transient time in the inductive load case and two alternations of the 4 MHz input signal*

4.2.4 Maximum power point tracking

The power output of a photovoltaic panel can vary with weather factors such as temperature, illumination, and shading. In such context, the output of the photovoltaic panel has to be adapted to those conditions in order to extract the maximum of power. Furthermore, adaptation between load variations and PV outputs (voltage and current) is required to keep the delivered power at its maximum point. This maximum is called the maximum power point (MPP) and the process of this continuous adaptation is referred to as maximum power point tracking MPPT [26-28].

The MPPT is effectuated by means of power DC-DC converters, in which the control, generally, is carried out through algorithms that continually controls gates of power converter switches. Figure 4.12 represents the MPPT concept.

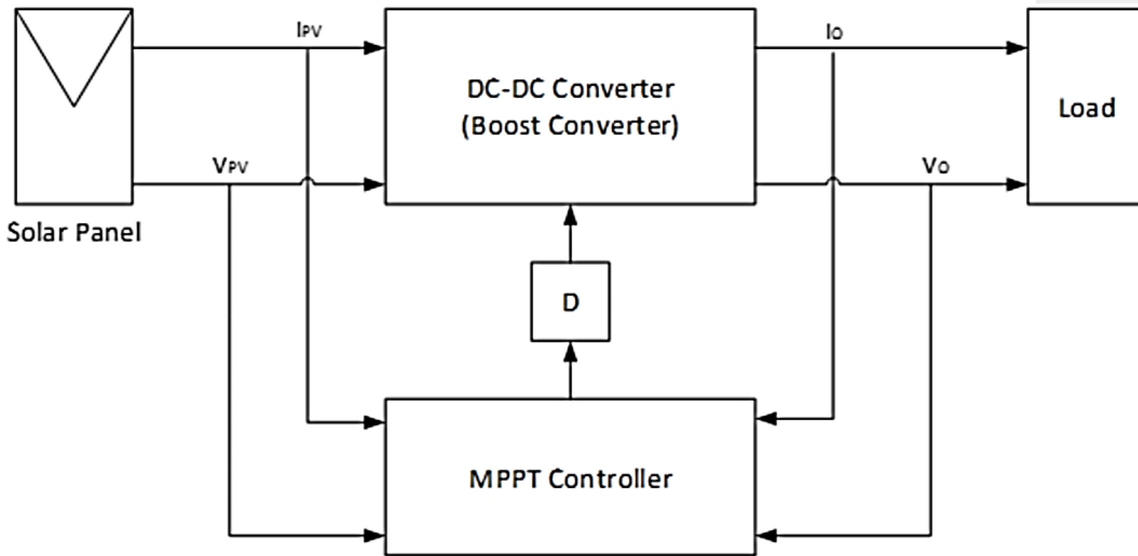


Figure 4.12 *Schematic of the MPPT concept*

Since the control of gates of power converter switches is at the core of the MPPT process, these switches performances are the basis of its efficiency. Thus, MPPT improvement could be realized through software optimization as well as through hardware optimization, and while most efforts are offered to the software side, our contribution is on the hardware side. More specifically, both the DC-DC boost and buck converters operating mode relies on the charging and the discharging of an inductance [29]. In fact, this operation is exactly what we have shown in the previous subsection, where we have demonstrated the improved performance of our proposed device with respect to its conventional counterpart. Therefore, it can be derived from the previous chapter and subsections that the strategic combination between both JL and gate-trench aspects can enable achieving enhanced electrical, and switching performances in power conversion circuits. Consequently, we believe that the proposed device can be suitable for the development of efficient and low-cost power electronic systems such as DC-DC converters for photovoltaic MPPT.

4.3 Conclusion

In the first part of this chapter, we have demonstrated that the device power performances can be improved using an intermediate high-k dielectric layer between silicon dioxide and the gate electrode. In this context, an improvement in the breakdown voltage has been observed by using high-k materials jointly with the oxide in comparison with the oxide alone. We have shown also that the increase of the gate dielectric thickness can alter the breakdown voltage, but with the increase of the permittivity the breakdown voltage preserves a stable behavior against the increase of the thickness until a certain limit. Furthermore, the addition of high-k materials results in alleviation of the quasi-saturation regime and increase of the gate controllability. In the second part, we have shown that the switching performances of our proposed junctionless trench gate MOSFET surpass those of its conventional counterpart for both resistive loads and inductive loads on a circuit level analysis. Our findings are highly suggestive of the improvements that might be provided by the adoption of our proposed approach in power devices for power electronics applications such as DC-DC converters in photovoltaic systems.

4.4 References

[1] B. J Baliga, 2008, Fundamentals of Power Semiconductor Devices, Springer, New York, USA.

[2] T. Hosoi et al. Performance and Reliability Improvement in SiC Power MOSFETs by implementing AlON high-k gate dielectrics. in Dig. IEEE Int. Electron Devices Meeting, San Francisco, CA, USA, 159–162, 2012.

[3] R. Djamil, K. Aicha., A. Cherifa and F. Djeffal (2016, October). Impacts of high-k gate dielectrics and low temperature on the performance of nanoscale CNTFETs. Journal of Computational Electronics, 15(3), 1308-1315.

[4] M. Huang and X. Chen. Theory of an improved vertical power MOSFET using high-kinsulator. Superlattices and Microstructures, 88(1), 244-253, 2015.

[5] J. Yao, Y. Guo, T. Xia and J. Zhang. Hong Lin 3D analytical model for the SOI LDMOS with alternating silicon and high-k dielectric pillars. Superlattices and Microstructures, 96(1), 95-103, 2016.

[6] H. Wong, H. Iwai. On the Scaling Issues and High-k Replacement of Ultrathin Gate Dielectric for Nanoscale MOS Transistor," Microelectronic Engineering. Microelectronic Engineering, 83(3), 1867-1904, 2006.

[7] A. Galadi. Accurate power MOSFET models including quasi-saturation effect. Journal of Computational Electronics, 15(3), 619-626, 2016.

[8] N.P. Maity, A. Pandey, S. Chakraborty, M. Roy. high-k HfO2 based metal-oxide-semiconductor devices using silicon and silicon carbide semiconductor. J. Nano-Electron. Phys, 3(3), 947-955, 2011.

[9] B. J Baliga, Advanced Power MOSFET Concepts, Springer Press, USA, 2010.

[10] A Z. M. LI, P. A. Mawby, K. Board. A physical insight into the quasi- saturation effect in VDMOS power transistors, Int. J. Electronics, 83(3), 13-22, 1997.

[11] E. Kuffel, W. S. Zaengl, J. Kuffel. High Voltage Engineering fundamentals. Newnes, Britain, 2000.

[12] J. Lutz, H. Schlangenotto, U. Scheuermann, R. D. Doncker. Semiconductor Power Devices, Springer, Berlin, Germany, 2011.

[13] W. J. Schäfer, G. H. Negley, K. G. Irvin, J. W. Palmour. Conductivity anisotropy in epitaxial 6H and 4H SiC. Proceedings of Material Res. Society Symposium, 339(3), 595-600, 1994.

[14] S. Selberherr. Analysis and Simulation of Semiconductor Devices. Springer-Verlag, Wien-New York, USA, 1984

[15] Lombardi et al. A Physically Based Mobility Model for Numerical Simulation of Non-Planar Devices. IEEE Trans. on CAD, 7(3), 1164-1171, 1988.

[16] F. Djeffal and N. Lakhdar. An improved analog electrical performance of submicron Dual-Material gate (DM) GaAs-MESFETs using multi-objective computation. Journal of Computational Electronics, 12(3), 29-35, 2013.

[17] M. A. Abdi, F. Djeffal, Z. Dibi, D. Arar. A two-dimensional analytical subthreshold behavior analysis including hot-carrier effect for nanoscale Gate Stack Gate All Around (GASGAA) MOSFETs. Journal of Computational Electronics, 10(3), 179–185, 2011.

[18] T. Bentrcia, F. Djeffal and A. Benhaya. Continuous analytic I—V model for GS DG MOSFETs including hot-carrier degradation effects. Journal of Semiconductors, 33(3), 014001-1- 014001-6, 2012.

[19] H. Ferhati and F. Djeffal. Role of Optimized Grooves Surface -Textured Front Glass in improving TiO2 Thin Film UV Photodetector Performance. IEEE sensors journal, 16(3), 5618-5624, 2016.

[20] Yongheng Yang, et al. Advances in Grid-Connected Photovoltaic Power Conversion Systems. Elsevier press, 2019.

[21] Ramadan, F. Z., Djeffal, F., Drissi, L. B., Saidi, S., & Ferhati, H. Highly efficient ACdTS kesterite solar cell based on a new photovoltaic material. Journal of Physics and Chemistry of Solids, 161, 110458, 2022.

[22] Ferhati, H., Djeffal, F., Boubiche, N., Benhaya, A., Faerber, J., Le Normand, et al. Absorption enhancement in amorphous Si by introducing RF sputtered Ti intermediate layers for photovoltaic applications, vol. 269, 115152, 2021.

[23] H. Ferhati, F. Djeffal and L. B. Drissi, A new approach to the modeling and simulation of multi-junction solar cells, Optik vol. 200, pp.163452, 2020.

[24] H Ferhati, F Djeffal, BL Drissi. Performance improvement of Perovskite/CZTS tandem solar cell using low-cost ZnS/Ag/ITO multilayer spectrum splitter, Superlattices and Microstructures, vol. 148, 106727, 2020.

[25] B Zerroumda, H Ferhati, F Djeffal, S Benaggoune. A novel high-performance junctionless 4H-SiC trench MOSFET with improved switching characteristics. Microelectronic Engineering, vol. 277, pp. 112011, 2023.

[26] Shuangming Duan, et al. Design of Photovoltaic Power Generation MPPT Controller Based on SiC MOSFET. IEEE Region 10 Conference, pp. 1-5, 2015.

[27] Venkata R. Vakacharla, et al. State-of-the-art power electronics systems for solar-to-grid Integration. Solar energy, 210, pp. 128-148, 2020.

[28] Md. Rabiul Islam, et al. State-of-the-Art of the Medium-Voltage Power Converter Technologies for Grid Integration of Solar Photovoltaic Power Plants. IEEE Transactions on Energy Conversion, Vol. 34, pp. 372-384, 2019.

[29] Francesco Iannuzzo. Modern Power Electronic Devices: Physics, Application and reliability. IET press, 2020.

General Conclusion

Conclusion and future prospects

Our work in this dissertation was built around design, modeling and optimization of power devices intended for power electronics applications, knowing that wide bandgap-based power devices are all about the future of power electronics. Particularly, SiC-based power devices are reaching a level of unmatched technological maturity among all power devices based on wide bandgap materials. Undoubtedly, 4H-SiC MOSFET is the most important commercially available silicon carbide power device. Accordingly, we have been able, following a thorough analysis, to locate a problematic regarding power SiC MOSFETs, which is the SiC/SiO_2 interface poor quality hindering the series resistance of SiC-MOSFETs and the threshold voltage stability. In addition, lays the high fabrication cost of silicon carbide power MOSFET in comparison to silicon IGBT, which is still the dominant discreet power device in the market. Actually, the problem with the cost starts from the expensive growth process of silicon carbide including very high temperatures and different dopants. Besides, the use of complicated structures with several abrupt junctions can further increase the fabrication cost.

This compound problematic is the root cause behind many performance limitations, reliability restrictions, and high cost issues. Along this dissertation, we have carried out an extensive work aiming at resolving this problematic from the conceptual level. Such work was based on bringing about innovative yet pertinent solutions, which practically can introduce improvements to the SiC-MOSFET from the very beginning until the moment the device is implemented into power circuits. From a physical point of view, we have tried to propose a device, which has the ability to carry a volume current under the gate instead of the sheet current resulting from the inversion layer in all conventional power MOSFETs with pn junctions.

Such solution would be beneficial for the mobility, because it would be a mobility of majority carriers instead of a mobility of inversion carriers. Furthermore, in such case we would be successful in reducing the hindering effects of the SiC/SiO_2 interface by giving the charge carriers another dimension to stay away from the interface or at least circumvent the close contact with it. Most importantly, the elaboration of this solution relieves the budget of the very expensive enhancement of the SiC/SiO_2 by growth processes, and surprisingly, it is less expensive than the elaboration of a conventional pn junction power MOSFET.

To that extent, the accomplished scientific research in this dissertation was initiated from the materials description in the first chapter, where we have presented two sets of materials, the SiC

family, and the III-nitrides family, together with gallium oxide. The SiC electrical and crystal properties provide a basis for the employment of SiC in the modeling of SiC-MOSFETs in this dissertation, and a justification for the choice of this material. Furthermore, the III-nitrides properties is demonstrated as they are the most important SiC competitors in both the scientific research and the industry. Regarding gallium oxide, it represents a new set of ultra-wide bandgap materials.

In this light, the only limitation to the wide spread adoption of silicon carbide in power devices is the high cost of its fabrication compared to silicon. Regarding III-nitrides, they are commercially available as epilayer materials, and they are widely endorsed in power RF applications. However, the full potential of these materials cannot be achieved until a mature cost-effective technology of their native bulk growth is available. Following the same logic, wide bandgap-based devices and power converters are discussed, as they represent the domain of application to our strategy.

In the second chapter, we have proposed the first innovative realization of our strategy, which was a planar power MOSFET based on the Junctionless concept. The main idea behind the proposed device dwells on introduced symmetrical oxide regions based on grooves-like shape instead of two P-bases regions to develop a JL structure. This device was investigated and compared to its conventional counterpart using accurate numerical models. It was shown that the proposed structure exhibits an enhanced breakdown behavior as compared to its conventional counterpart, as it demonstrates a great ability to support higher critical electric fields, in addition to preserving a good agreement with the specific on-resistance, which was expressed by a superior figure of merit. This is attributed to the elimination of the hindering effect of the channel mobility. Furthermore, it is shown that the use of the JL structure allows modulating device threshold characteristics, where the proposed JL device exhibits a lower threshold voltage of 1.1 V as compared to the conventional structure 2.2 V. An analysis of the effect of the trench oxide dimensions on the drain current and breakdown characteristics has been carried out and thoroughly discussed. This feature of variable oxide dimensions allows the proposed structure to be adaptable to a variety of applications in which the saturation regime and the linear regime play different roles in each case. Those significant results makes the proposed JL structure a promising cost-effective strategy toward the design of high-performance planar 4H-SiC MOSFETs, which are highly suitable for power integrated devices compared to trench MOSFETs.

In the third chapter, we have combined the junctionless concept with the gate trench structure which has yielded a novel SiC power MOSFET device. This proposed device was investigated physically, electrically, and geometrically by developing accurate numerical models. As expected, this device has exhibited low threshold voltage. In addition, it is found that the proposed SiC trench power MOSFET with JL aspect exhibits low energy loss and superior switching speed as compared to its conventional counterpart, providing reduced ON-resistance of 1.6 $m\Omega/cm^2$ and lower HF-FoM of 1078 mΩ.pF. Moreover, it demonstrates superior breakdown properties with a high BV exceeding 2 kV and a high FoM of 2580 $V^2/m\Omega.cm^{-2}$.

This outstanding result is attributed to its ability to support high critical electric field near the gate edge of 3.93 MV/cm, together with its improved series resistance. Therefore, we suggest that the presented study can offer new insights for the design of high-performance cost-effective SiC power MOSFET, which can be promising candidate for the emerging power systems.

The fourth chapter was divided into two parts. The first part shows the beneficial effects of the adoption of high-k materials on the device power performances. More specifically, improvements of the breakdown voltage have been observed by using high-k materials jointly with the oxide in comparison with the oxide alone. We have shown also that the increase of the gate dielectric permittivity has a compensatory effect regarding the increase of the dielectric thickness, which can alter the breakdown voltage. Furthermore, the addition of high-k materials results in alleviation of the quasi-saturation regime and increase of the gate controllability.

The second part of the fourth chapter, was dedicated to demonstrate the optimizations related to the application of the proposed trench junctionless SiC-MOSFET in an electrical circuit. It was found that the proposed junctionless trench SiC-MOSFET surpasses its conventional counterpart in terms of switching performances for both resistive loads and inductive loads on a circuit level analysis. Since boost converters functioning is based on charging and discharging of an inductance. Thereby, our findings are highly suggestive of the improvements that might be provided by the adoption of our proposed approach in power devices for power electronics applications such as DC-DC converters in photovoltaic systems.

As future prospects, we think that it is worthy to implement the proposed devices along this dissertation in more complicated power electronic circuits realized in Pspice environment. In addition, we believe that new figures of merit should be investigated to shed light on other aspects of the proposed strategy.

Intuitively, further enhancements are possible by optimizing the device structure. Accordingly, metaheuristic optimization techniques based on genetic algorithm and particle swarm methods can be used for selecting the most appropriate design configuration, providing the highest FoMs for power electronics applications.

Although power devices fabrication is regarded as a very meticulous and laborious scientific task, which requires adequate experimental establishments and abundant funding. We believe that the elaboration of prototypes of the proposed devices could be within the realm of our future work.