République Algérienne Démocratique et Populaire
Ministère de l'Enseignement Supérieur et de la Recherche Scientifique

Université Batna 2 – Mostefa Ben Boulaïd
Faculté de Technologie
Département d'Électronique

Thèse

Préparée au sein du Laboratoire d'Electronique Avancée (LEA)

Présentée pour l'obtention du diplôme de :

Doctorat en Sciences en Électronique
Option : Microélectronique

Sous le Thème :

Contribution to the modeling and optimization of nanoscale VSG MOSFETs : Application to the nanoscale circuits design

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Décembre 2018

Acknowledgements

First of all, I thank ALLAH almighty who armed me with determination, patience and courage during all these years of study.

I would like to express my sincere gratitude to my adviser, Pr. Fayçal DJEFFAL, for his solid technical guidance, continuous support and encouragement in my work and for his responsiveness to my requests.

I am also grateful to Pr. Abdesselam HOCINI and Pr. Djamel KHEDROUCHE, who accepted to be my jury members, and devoted their precious time to review my thesis. I also want to thank Pr. Abdelhamid BENHAYA for having agreed to preside this jury.

I would like to thank Dr. Toufik BENTRCIA for his orientations and his judicious advice.

Finally, my deep recognition goes to my dear parents, Abdelhamid and Farida, for all their encouragements and continuous support during this period of research. My deep recognition goes to my late beloved grandmother Fatima.

A particular gratitude to my sister Dr. Ibtissem ABDELMALEK and her Husband Pr. Nabil BENOUDJIT, for their advice, moral support and encouragements. I am also grateful to all my family, especially my brother Hachemi and my sister Ahlem. I also would like to thank my friend Hamza AZZA for his support. Once again thanks for all.

Abstract

In this dissertation, a contribution to the study, modeling and reliability evaluation of advanced MOSFET devices is presented. The focus is made on two devices, identified as a potential solution for the near future scaling and integration technology, namely the tunnel and junctionless field effect transistors (TFET and JLFET). An insight on the transport physics permits a comprehensive study of the devices' characteristics and performances.

A continuous and accurate model based on two-dimensional potential solution of an undoped tunnel transistor in vertical surrounding gate structure (VSG-TFET) is proposed. The continuity of the developed model provides the possibility to extract the analog/RF parameters and the device figures of merit (FOMs). Moreover, the role of introducing a high-κ layer on the gate oxide in improving the VSG-TFET behavior is explored for high-performance analog/RF applications. The proposed continuous analytical model can be easily implemented in commercial simulators to study and investigate VSG-TFET-based nanoelectronic circuits.

A semi-analytical model of an undoped heterojunction tunnel transistor in vertical surrounding gate structure (VSG-TFET) is developed. Basing on nonlocal approach and using an appropriate set of the wavevectors and region contribution, the tunneling current expression is derived. The model is calibrated and validated by two-dimensional numerical simulations. The impact of materials composition, dimensions and voltage supplies on the device performances is investigated and clarified. Terminal capacitances expressions complete the core model that is then used for the optimization of the device at circuit level. Design rules for heterojunction TFET based digital and analog/RF applications are outlined.

The JLFET reliability is investigated. A comparative evaluation of the hot carrier degradation (HCD) in VSG-JLFET and equivalent inversion mode device is proposed. The study focuses on the interface states creation by hot electron injection (HEI). Basing on the evolution of the interface states spatial distribution with extended stress time, and using the amphoteric property of the traps, an assessment of the aging phenomenon on various devices' parameters is performed. The evaluation of HCD on static and dynamic operation of both device types in CMOS inverter configuration is carried out.

Keywords: Vertical surrounding-gate, Tunneling FET, Heterojunction, Junctionless FET, Continuous modeling, Analog/RF, Hot carrier degradation, Circuit reliability.

Résumé

Dans cette thèse, une contribution à l'étude, la modélisation et l'évaluation de la fiabilité des dispositifs MOSFETs avancés est présentée. L'effort est centré sur deux dispositifs, identifiés comme une solution potentielle pour les mise à l'échelle et technologie d'intégration dans un futur proche, à savoir les transistors à effet tunnel et sans-jonction à effet de champ (TFET et JLFET). Un aperçu de la physique des transports permet une étude complète des caractéristiques et des performances des dispositifs.

Un modèle continu et précis basé sur la solution 2-D du potentiel d'un transistor à effet tunnel non dopée dans une structure verticale à grille enrobé (VSG-TFET) est proposé. La continuité du modèle proposé offre la possibilité d'extraire les paramètres analogiques/RF ainsi que les facteurs de mérite du composant (FOM). De plus, le rôle de l'introduction d'une couche à haute permittivité dans l'oxyde de grille dans l'amélioration du comportement du VSG-TFET est exploré pour des applications analogiques/RF hautes performances. Le modèle analytique continu proposé peut être facilement implémenté dans des simulateurs commerciaux afin d'étudier et d'explorer les circuits nanoélectroniques basés sur le VSG-TFET.

Un modèle semi-analytique d'un transistor tunnel à hétérojonction non dopé dans une structure verticale à grille enrobé (VSG-TFET) est développé. L'expression du courant tunnel est dérivée en se basant sur une approche non locale et en utilisant un ensemble approprié des contributions des vecteurs d'onde et région de transmission. Le modèle est calibré et validé par des simulations numériques à deux dimensions. L'impact de la composition des matériaux, des dimensions et des tensions d'alimentation sur les performances du dispositif est étudié et clarifié. Les expressions de capacités des terminaux permettent de compléter le modèle de base, servant par la suite à optimiser le dispositif au niveau du circuit. Des règles de conception sont formulées pour les applications numériques et analogiques/RF à base de TFET à hétérojonction.

La fiabilité du JLFET est étudiée. Une évaluation comparative de la dégradation induite par les porteurs chauds (HCD) dans le VSG-JLFET et un dispositif équivalent à mode d'inversion est proposée. L'étude porte sur la création d'états d'interface par injection d'électrons à chaud (HEI). En se basant sur l'évolution de la distribution spatiale des états d'interface pour un temps de contrainte étendu, et en utilisant la propriété amphotère des pièges, une évaluation du phénomène de vieillissement sur les divers paramètres des dispositifs est effectuée. L'évaluation de la HCD sur le fonctionnement statique et dynamique des deux types de dispositifs dans une configuration d'inverseur CMOS est menée.

Mots Clés: Structure verticale à grille enrobé, Transistor à effet tunnel, hétérojonction ,Transistor sans jonction, modèle continu, analogique/RF, Dégradation induite par les porteurs chauds, Fiabilité des circuits.

ملخص

في هذه الأطروحة، يتم تقديم مساهمة في دراسة، نمذجة و تقييم موثوقية بنيات MOSFET المتقدمة. يتم التركيز على بنيتين، حددتا كحل محتمل لتكنولوجيا التحجيم و الدمج في المستقبل القريب، وهما الترانزستورات الحقلية ذات تأثير نفقي و بدون وصائل (TFET و JLFET). تسمح نظرة عامة في فيزياء النقل بإجراء دراسة شاملة لخصائص البنيات وأداءها.

يقترح نموذج مستمر ودقيق قائم على حل ثنائي الأبعاد للتوزيع الالكتروستاتيكي لترانزستور ذي تأثير نفقي بدون تشويب في بنية عمودية ذات بوابة اسطوانية (VSG-TFET). توفر استمرارية النموذج المقترح إمكانية استخراج المعلمات التناظرية/ترددات الراديو وأرقام الجدارة (FOMs). وعلاوة على ذلك، يتم استكشاف دور إدخال طبقة عالية السماحية على أكسيد البوابة في تحسين أداء VSG-TFET للتطبيقات التناظرية/ترددات الراديو عالية الفعالية. يمكن إدراج النموذج التحليلي المستمر المقترح بسهولة في أدوات المحاكاة التجارية للدراسة و التحقق من دوائر النانو الإلكترونية التي تعتمد على VSG-TFET.

يتم تطوير نموذج شبه تحليلي لترانزستور ذي تأثير نفقي غير متجانس بدون تشويب في بنية عمودية ذات بوابة اسطوانية (VSG-TFET). استنادًا إلى النهج غير المحلي وباستخدام مجموعة مناسبة لمساهمة شعاع الموجات و مناطق الانتقال، يتم اشتقاق التعبير للتيار النفق. يتم معايرة النموذج والتحقق من صحته بواسطة محاكاة رقمية ثنائية الأبعاد. يتم دراسة وتوضيح تأثير تركيبة المواد والأبعاد ومستلزمات الجهد على أداء البنية. تكمل تعابير السعة النموذج الأساسي الذي يتم استخدامه بعد ذلك لتجويد البنية على مستوى الدوائر الكهربائية. يتم اقتراح قواعد التصميم من أجل التطبيقات الرقمية و التناظرية/ترددات الراديو القائمة على TFET غير متجانس.

يتم التحقيق في موثوقية JLFET. يتم إجراء تقييم مقارن للتدهور الناتج عن الحامل الساخن (HCD) في بنية VSG-JLFET وبنية وضع معكوس. تتركز الدراسة على إنشاء حالات السطح البيني عن طريق حقن الإلكترون الساخن (HEI). بالاستناد إلى تطور التوزيع المكاني لحالات السطح البيني مع امتداد زمن الإجهاد، وباستخدام الخاصية المذبذبة للمصائد، يتم إجراء تقييم لظاهرة الشيخوخة على مختلف خصائص البنيات. يتم إجراء تقييم HCD على التشغيل الثابت والديناميكي لكلا النوعين من البنيات في تشكيلة عاكس CMOS.

الكلمات الدالة: بنية عمودية ذات بوابة اسطوانية، ترانزستور ذو تأثير نفقي، وصلة غير متجانسة، ترانزستور بدون وصائل، نمذجة مستمرة، تناظرية/ترددات الراديو، التدهور الناتج عن الحامل الساخن، موثوقية الدوائر.

Contents

1. Introduction and state of the art

From the fabrication of the first Intel microprocessor in 1971 to the first 1 terabyte memory card in 2016, the electronic industry has seen an extraordinary evolution. This technological progress was carried by the aggressive integration, new architectures, alternative materials, process development and mostly by the tremendous efforts of electrical engineers and researchers. In 1965 Gordon Moore presented his theory on the evolution of transistors' density in integrated circuits, he predicted that the number of transistor per chip will double every two years, which became the "Moore's law", law governing the roadmap and the line of objectives, which has been very well followed by the semiconductor industry throughout the next forty years [1]. In this race of integration, the biggest manufacturers created the International Technology Roadmap for Semiconductors (ITRS), an organization whose goal is to guarantee the cost-effectiveness of the progress made in the realization of integrated circuits and a more accurate prediction of the future of the semiconductor industry [2]. Until recently, the downscaling of transistors has generally followed simple but strict design rules with slight modifications. These rules dictates that the reduction of the length of a transistor must be accompanied by a reduction of several other physical, geometrical and electrical parameters relative to a common factor, and this to ensure an improvement of circuits' speed, density and energy consumption, while preserving electrostatic reliability and integrity [1].

However, after several years of racing towards miniaturization and approaching the submicron scale, the designers were confronted with new problems that are no longer limited to the technical difficulties of realization. New phenomena have emerged, putting into question physics and design models. Among these undesirable effects those related to channel length reduction known as short channel effects (SCEs), such as the drain induced barrier lowering (DIBL), the subthreshold slope (SS) degradation and the threshold voltage roll-off. These phenomena result in a rise of the off-state and gate leakage currents which increase the passive power consumption. Collected data form literature show that the passive power density, either in subthreshold regime or that induced by the gate leakage current, increases in a spectacular manner and becomes the dominant part of the total power density as depicted in fig 1.1 [3].

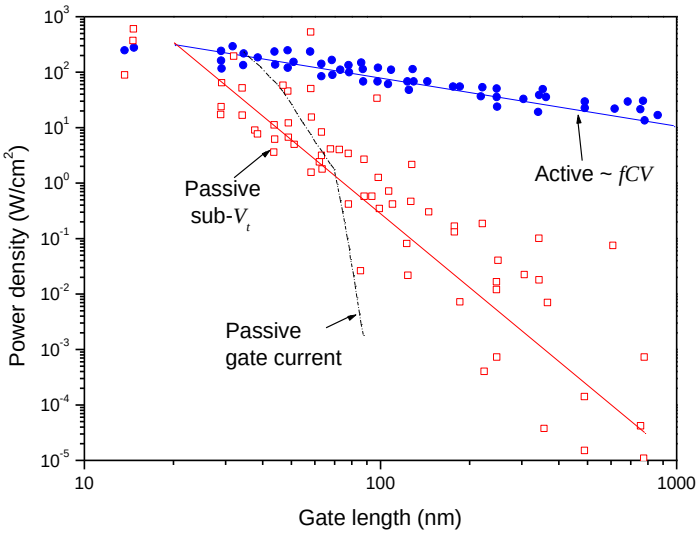

Figure 1.1 – Active and passive power density evolution with scaling CMOS technologies from 1 µm to 65 nm. Lines show the scaling trend. Data from [3]

Silicon-on-insulator (SOI), multigates structures, high-κ dielectric oxide, doping engineering and lithography evolution allowed extending the scaling to few nanometers decades. The resulting electrostatic controllability enhancement permits a sensible improvement of the SS and a reduction of gate and channel leakage currents. Nevertheless, the physical gate length as well as the drain supply scaling reached a critical limit and further reduction implied the investigation of new devices based on different physics that can overcome the Boltzmann limit of 60 mV/dec at room temperature. The SS can be expressed as:

$$SS = \underbrace{\frac{dV_{gs}}{d\psi_s}}_{m} \underbrace{\frac{d\psi_s}{d(\log I_d)}}_{n}$$

where ψ_s represents the surface potential, V_{gs} the gate voltage and I_d the drain current. m is the body factor and n refers to the Boltzmann limit. Therefore, to achieve steep SS, two solutions are available. The first one consists in the reduction of the body factor. The reduction of the oxide thickness or the use of high-κ materials yields in the best case a body factor approaching 1. A better way is to exploit internal amplification mechanisms that yield

a negative capacitance (NC) and reduce the body factor below 1. Ferroelectric materials that can provide such NC with the dielectric polarization produce voltage amplification while the impact ionization (II) yields current amplification. The second solution is based on different transport mechanisms that can result in sub-60 mV/dec. In this field, tunnel field effect transistor (TFET), nanoelectromechanical (NEM) relay and phase change switches show the ability to overcome the Boltzmann limit [4].

Intensive researches are currently going on to find which device can offer the best compromise between performance, scaling capability, reliability and cost, all the more that the electronic industry operated a reorientation toward smartphones, wireless devices, sensors, artificial intelligence, internet of things and data centers. In this context, a restructuration of the roadmap was initiated and was replaced by the ITRS 2.0 [5]. Soon after, an all-new international roadmap for devices and systems (IRDS) was launched [6]. Aligned with the previous efforts, this roadmap focuses on matters such as More Moore, Beyond CMOS and Outside System Connectivity. New benchmarking methodologies are proposed to fulfill the beyond-CMOS perspective [7]. A study that focused on novel devices for Boolean and non-Boolean logic applications clearly identified the TFET as the best candidate for low power, high speed application as showcased in fig 1.2.

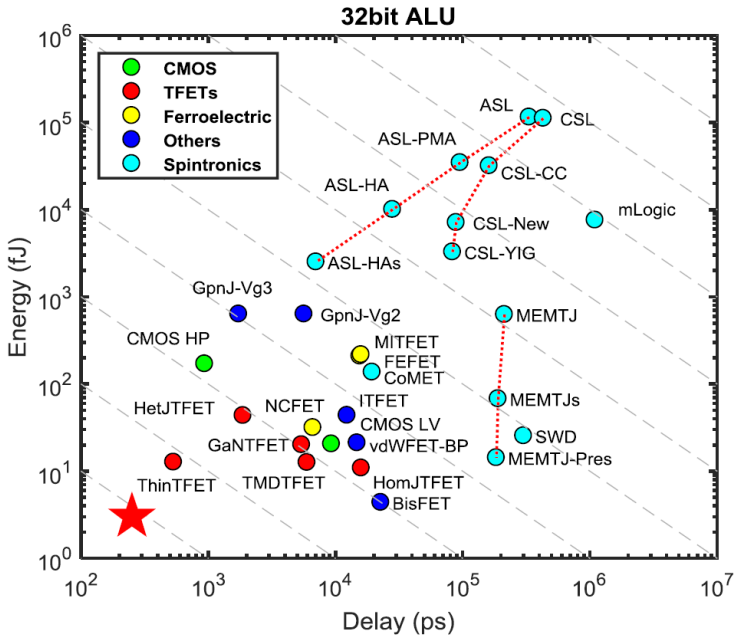

Figure 1.2 – Energy versus delay plot of 32bit ALU built from benchmarked devices [7]

TFET is considered as emerging logic device and a potential alternative for future high-performance and low power processor chips [5, 6]. Experiments show the viability of complementary TFET architecture [8], where a fully functional low power Si GAA NWTFET inverter with suppressed ambipolarity and large noise margin was fabricated. The electrostatic control enhancement of gate all around structure compared to planar TFETs was demonstrated [9]. Generally, this device is characterized with low leakage current, steep subthreshold slope, efficient transconductance and high intrinsic gain. Experiments and studies exhibit also the potential of tunneling transistors for low power amplification, analog/RF and sensing applications [8-11]. At circuit level, new various heterogeneous CMOS-TFET designs with different reliability issues are investigated [10, 12]. Also, TFETs have better immunity against SCEs than conventional MOSFETs above 30 nm [13, 14]. Moreover, III-V, narrow bandgap and strained materials were and are still intensively investigated as performance booster to overcome the low on-current provided by Si and wide bandgap materials. However, a narrow bandgap implies also an enhancement of the ambipolar and off-state currents [15-17]. Heterojunction TFETs were then introduced as a device that can relate between the low power and high performance requirements and even surpass conventional MOSFETs [18]. Heterojunction TFETs fabrication is still challenging and must take into account the problematic lattice mismatch and junction interface defects that enhance the off-current and degrade the subthreshold slope [11]. On the other hand, compact and continuous models that could be applied to both subthreshold and superthreshold working domain are useful for understanding both device types and for circuit simulation. Also, accurate Heterojunction TFET models would simplify the exploration of the large available possibilities provided by compounds and alloys composition. This field is steel subject to concentrated efforts and a lake of efficient TFET models is noticed.

Moreover, the downside of the successful downscaling is the increase of technology cost. Indeed, intensive researches had to be made for every new technology node along with the development of new high precision lithography masks and techniques. The increasing effect of the impurities diffusion from the extensions into the channel yields a serious reliability issue and implies the use of additional costly annealing techniques [19]. Therefore, the junctionless transistor (JLFET) was proposed as a simple and practical solution [20]. With a uniform one type doping over the entire device, the JLFET first fabricated by Colinge *et al*

[19] showed good switching properties and puts paid to the notion that the major mobility degradation due to the high body doping will result in poor characteristics. The device demonstrates a very high scaling capability with its improved immunity against SCEs resulting from the absence of junctions [21]. Although a relative underperformance is characterized in comparison with inversion mode MOSFETs (lower on-current, transconductance, cutoff frequency), the device fulfills the actual and projected roadmap requirements for low power and high performance applications [6].

Transistors reliability represents a major issue of the ultra large scaling. MOSFET degradation is well known and was largely studied over the past decades [22]. This degradation is directly related to the increase of the electric field that results from the dimensions reduction and the thinning of the oxide layer. Channel hot carrier and hot carrier injection were identified as responsible of interface states and oxide traps creation [22, 23]. The JLFET suffers from the same reliability issues identified in MOSFETs. A subsequent degradation of all the metrics is observed. Nevertheless, experiments demonstrate that the JLFET show less degradation than conventional inversion mode devices [24, 25]. Therefore, an in-depth study of the interface state creation and the induced performances degradation that can explain this enhanced immunity is suitable. Also, this study represents an essential step for the development of new compact models that includes the hot carrier degradation, and thus in the aim of allowing a robust prediction of the large circuits' aging process [26].

Moreover, the IRDS roadmap projects the introduction of lateral GAA structure for logic devices technology for 2019. An evolution to vertical GAA structure is expected for 2021. Such structure would allow for vertical devices stacking and monolithic 3-D (M3D) integration yielding higher integration density, lower interconnect parasitics and permitting lower operating voltage [6, 27]. Also, the successful fabrication by epitaxial growth of both tunnel and JL nanowire vertical transistors paves the way to the incorporation of these devices in future integrated circuits [28, 29].

In this context, our work brings a modest contribution to study, modeling and reliability assessment of the TFET and JLFET in VSG structure. The main contributions can be recapitulated in what follows:

- A comprehensive study of both TFET and JLFET devices is presented ongoing from operating principles to characteristics and performances;
- The development of a continuous semi-analytical model of undoped VSG-TFET is conducted in a rigorous manner to account for various practical constraints;
- The RF/analog performances of silicon based VSG-TFET are investigated numerically and analytically in order to showcase the range of validity of the proposed models;
- The elaboration of a semi-analytical model of undoped heterojunction VSG-TFET is proposed in order to gain more insights regarding the device behavior;
- The impact of material definition and band alignment on the heterojunction VSG-TFET performances is investigated and elucidated;
- The genetic algorithm optimization is used to outline new design rules for heterojunction VSG-TFET based digital and analog/RF applications;
- An analysis of the interface traps creation, spatial distribution and evolution in time domain on both JL and IM VSG-MOSFET is performed in order to compare the induced degradation effects on both devices metrics;
- An assessment and elucidation of the hot carrier induced degradation on static and dynamic operation of CMOS inverter based on the two types of device is carried out.

Thesis outline

In chapter 2, a physical insight on the theory of tunneling in semiconductors is introduced along with the most widely used semi-classical models. This essential step allows us to develop a full comprehension of the TFET operation. The device characteristics are evaluated and compared with conventional MOSEFTs. The different possible structures are investigated. On the other hand, the semi-classical modeling of tunneling allows targeting the TFET limits, as well as the possible leads to the device parameters enhancement in order to match the low power and high performance MOSFET requirements identified in the technology roadmap. The possible solutions are investigated basing on recent experiments and simulations.

In chapter 3, a continuous and accurate model based on 2-D potential solution of an undoped vertical surrounding gate structure (VSG-TFET) is proposed. Both ambipolarity and dual modulation effects are included for more accurate analytical modeling of the device,

where the validity of this model is demonstrated by comparisons with two-dimensional numerical simulations using ATLAS- 2-D simulator. The continuity of the proposed model provides the possibility to extract the analog/RF parameters and the device figures of merit (FOMs). Moreover, the role of introducing a high-κ layer on the gate oxide in improving the VSG-TFET behavior is explored for high-performance analog/RF applications. The proposed continuous analytical model can be easily implemented in commercial simulators to study and investigate VSG-TFET-based nanoelectronic circuits.

In chapter 4, a semi-analytical model of undoped heterostructure VSG-TFET is presented. In the purpose of reaching a wide range of validity and applicability to various heterostructures, the model is elaborated on the basis of nonlocal tunneling approach that makes use of the band definition. Therefore, valid 2-D potential expressions are derived for the all device regions using both Boltzmann and Fermi-Dirac statistics and accounting for the extensions depletion, fringing fields and degeneracy. The drain modulation is also described as well as the ambipolar current which is essential to a reliable assessment of device performances. The heterostructure band alignment is calculated using the affinity rule. Following a nonlocal tunneling approach and using the WKB approximation, the proposed model yields encouraging results in both quantitative and qualitative aspects. Respectively, the model is calibrated and validated using ATLAS- 2-D simulator. An in-depth analysis of material composition, doping and dimensions impact on the device characteristics is also performed. Besides, terminals capacitances expressions are derived. Finally, by employing multi-objective genetic algorithms, the optimization of the device performances for both digital and analog application is carried out.

In chapter 5, after a short overview on the JLFET physics, a comparative evaluation of the hot carrier effect on the JLFET and IMFET performances degradation is carried out. This study is focused on the impact of the interface states created by hot electron injection. For this purpose, 2-D numerical simulations including Hänsch reliability model with the Tam lucky electron model are performed in order to extract the interface states profile. Instead of varying the interface traps density over a fixed distance as used in many studies, the extracted spatial distribution from the previous simulations is employed. Also, gaussian energetic distribution of the interface states is included in order to obtain a more realistic behavior of the traps' amphoteric nature. In addition to the evaluation of the hot carrier

degradation on many metrics, the impact on static and dynamic performances of CMOS inverter based on both types of device is investigated.

References

[1] H. R. Huff, “Into The Nano Era Moore's Law Beyond Planar Silicon CMOS,” Springer edition, Berlin, 2009.

[2] J.P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer edition, New York, USA,2008.

[3] W. Haensch, “Silicon CMOS devices beyond scaling,” IBM Journal of Research and Development, vol. 50, pp. 339-361, Jul. 2006.

[4] A. M. Ionescu, “Sub-unity body factor: The next CMOS and beyond CMOS technology booster for enhanced energy efficiency?,” Energy Efficient Electronic Systems & Steep Transistors Workshop (E3S), 2017 Fifth Berkeley Symposium on, Berkeley, CA, USA, 19-20 Oct. 2017.

[5] http://www.itrs2.net/

[6] https://irds.ieee.org/

[7] C. Pan, A. Naeemi, “An Expanded Benchmarking of Beyond-CMOS Devices Based on Boolean and Neuromorphic Representative Circuits,” IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 3, pp. 101-110, Dec. 2017.

[8] G. V. Luong, *et al*., “Complementary Strained Si GAA Nanowire TFET Inverter With Suppressed Ambipolarity,” IEEE Electron Device Letters, vol. 37, pp. 950-953, Aug. 2016.

[9] C. Schulte-Braucks, *et al*., “Experimental demonstration of improved analog device performance of nanowire-TFETs,” Solid-State Electronics, vol. 113, pp. 179-183, Nov. 2015.

[10] S. Datta, H. Liu, V. Narayanan, “Tunnel FET technology: A reliability perspective,” Microelectronics Reliability, vol. 54, pp. 861-874, May. 2014.

[11] A. C. Seabaugh, Q. Zhang, “Low-Voltage Tunnel Transistors for Beyond CMOS Logic,” Proceedings of the IEEE, vol. 98, pp. 2095-2110, Dec. 2010.

[12] D. Schmitt-Landsiedel, C. Werner, “Innovative devices for integrated circuits – A design perspective,” Solid-State Electronics, vol. 53, pp. 411-417, Apr. 2009.

[13] L. Liu, D. Mohata, S. Datta, “Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors,” IEEE Transactions on Electron Devices, vol. 59, pp. 902-908, Apr. 2012.

[14] N. D. Chien, C. H. Shih, “Short channel effects in tunnel field-effect transistors with different configurations of abrupt and graded Si/SiGe heterojunctions,” Superlattices and Microstructures, vol. 100, pp. 857-866, Dec. 2016.

[15] M. Najmzadeh, K. Boucart, W. Riess, A. M. Ionescu, “Asymmetrically strained all-silicon multi-gate n-Tunnel FETs,” Solid-State Electronics, vol. 54, pp. 935–941, Sep. 2010.

[16] F. Mayer, et al, “Impact of SOI, $Si_{1-x}Ge_xOI$ and GeOI substrates on CMOS compatible Tunnel FET performance,” IEEE International Electron Devices Meeting IEDM 2008, San Francisco, CA, USA, 15-17 Dec. 2008.

[17] S. Mookerjea, *et al.*, “Experimental demonstration of 100nm channel length $In_{0.53}Ga_{0.47}As$-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications,” in 2009 IEEE International Electron Devices Meeting (IEDM), pp. 1–3, IEEE, dec 2009.

[18] C. Convertino, *et al.*, “III–V heterostructure tunnel field-effect transistor,” Journal of Physics: Condensed Matter, vol. 30, pp. 264005, Jun. 2018.

[19] J. P. Colinge, *et al.*, “Nanowire transistors without junctions,” Nature Nanotechnology, vol. 5, pp. 225–229, Mar. 2010.

[20] C-W. Lee, *et al.*, “Junctionless multigate field-effect transistor,” Applied Physics Letters, vol. 94, pp. 053511(1-2), Feb. 2009.

[21] C. H. Park, *et al.*, “Electrical characteristics of 20-nm junctionless Si nanowire transistors,” Solid-State Electronics, vol. 73, pp. 7-10, Jul. 2012.

[22] E. Takeda, Hot-carrier effects in scaled MOS devices, Microelectronics Reliability, pp. 1687-1711, vol. 33, Sep. 1993.

[23] T. Grasser, Hot Carrier Degradation in Semiconductor Devices, Springer International Publishing, 2015.

[24] S. M. Lee, J. Y. Kim, C. G. Yu, J. T. Park, "A comparative study on hot carrier effects in inversion-mode and junctionless MuGFETs," Solid-State Electronics, vol. 79, pp. 253-257, Jan. 2013,

[25] C-H Park, *et al*., "Investigation on Hot Carrier Effects in n-type Short-Channel Junctionless Nanowire Transistors," Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on, Birmingham, UK, 20-23 Aug. 2012

[26] I. Sanchez Esqueda, H. J. Barnaby, M. P. King, "Compact Modeling of Total Ionizing Dose and Aging Effects in MOS Technologies," IEEE Transactions on Nuclear Science, vol. 62, pp. 1501-1515 , Aug. 2015.

[27] P. Chaourani, *et al*., Enabling area efficient RF ICs through monolithic 3D integration, Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017, Lausanne, Switzerland, 27-31 Mar. 2017.

[28] M. Hellenbrand, *et al*., Low-Frequency Noise in III–V Nanowire TFETs and MOSFETs, IEEE Electron Device Letters, vol. 38, pp. 1520-1523, Nov. 2017.

[29] L. Chen, F. Cai, U. Otuonye, W. D. Lu, "Vertical Ge/Si Core/Shell Nanowire Junctionless Transistor," Nano Letters, vol. 16, pp. 420-426, 2016.

CHAPTER2:

TFET, from theory to application

2.1. Introduction

Tunneling phenomena in semiconductor materials are well understood and efficiently modeled either in Zener diode, p-i-n junction or tunneling transistor, where several approaches have been proposed to investigate the quantum and tunnel transport mechanisms in the semiconductor devices [1-6]. The real interest on using the tunneling as the main transport mechanism in transistors came after the successful fabrication of the first steep subthreshold TFET [7]. Since then, many advances were made in the study, the modeling and the optimization of this device. TFET is now considered as an emerging logic device and a potential alternative for future high-performance and low power processor chips [8]. Experiments and studies exhibit the potential of tunneling transistors for low power amplification, logic devices, analog/RF and sensing applications [9-12].

Thus, a physical insight on the theory of tunneling in semiconductors is an essential step to the full comprehension of the TFET operation. On the other hand, the semi-classical modeling of tunneling allows targeting the TFET limits, as well as the possible leads to the device performance enhancement in order to match the low power MOSFET requirements identified in the technology roadmap. The possible solutions are investigated basing on recent experiments and simulations.

2.2. Tunneling theory

Tunneling effect is considered as a result of the dualistic property of electron. The Schrödinger wave function predicted that a particle could cross through a sufficient thin forbidden region from allowed region to another. In fact, an incident free particle of energy less than the height of a barrier should in classical physics be reflected. However, the consideration of a possible transmission associated with the continuity condition of the particle's wave function ψ at both sides of the barrier, implies an exponential decay of the wave function inside the forbidden region with the assumption that if this latter is sufficiently thin, the decay doesn't fall till vanishing so that a wave function of smaller amplitude is transmitted to the next region. Thus, it exist a finite probability of particle transmission through a barrier.

The first rigorous explanation of electron tunneling on its basis was made by Fowler and Nordheim [13] to describe electron emission in intense electric fields, leading to a one dimensional model that includes the effect of external field on the reduction of the barrier width and whose height equals the metal work function ϕ plus the Fermi energy E_f. The derived expression (2.1) of the current density as a function of electric field F well-known as Fowler-Nordheim formula was the premise of quantum tunneling theorization and modeling.

$$J = AF^2 \exp(-4\kappa\phi^{3/2} / 3F) \tag{2.1}$$

Soon after, in the study of the radioactive disintegration, the possibility of particle transmission through a wall was treated in the same manner of the Fowler-Nordheim approach (fig 2.1) [14]. The transmission probability is simply the ratio of the transmitted by the incident wavefunction probability densities. The developed model of the transmission probability was very similar to Fowler-Nordheim one's (2.2). Even if the previous authors did not explicitly use the tunneling term, their approach became the simplest examples to conceptualize and understand tunneling.

$$P(E) = A(E) \exp\left(4\pi / h \int \left[2m(V-E)\right]^{1/2} dx\right) \tag{2.2}$$

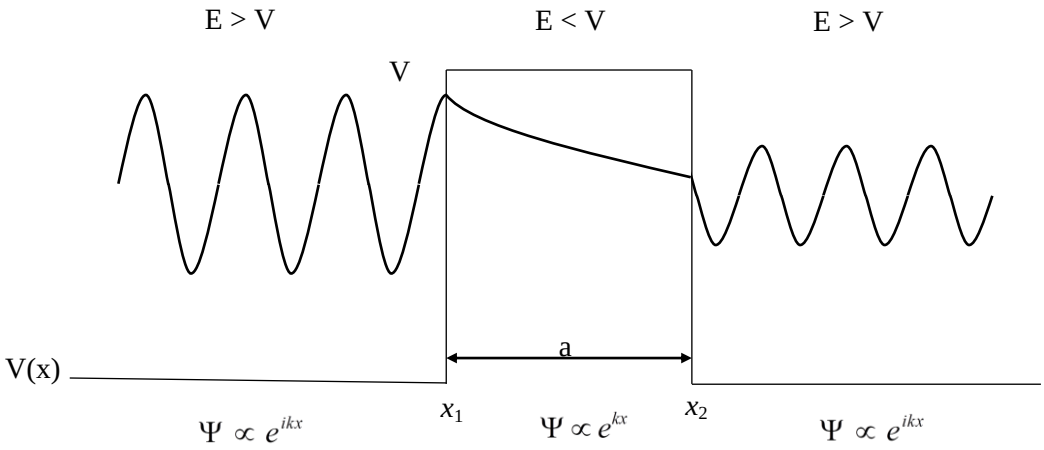

Figure 2.1 – Tunneling through a rectangular barrier.

In the case of more complex barrier profiles, the tunneling probability can be calculated using the WKB approximation, named after G. Wentzel, H. A. Kramers and L. Brillouin. This method gives the solution for the first order differential equation of the Schrödinger equation. Basically, this approach is made on the assumption of slow variation of the wave function amplitude and phase into the barrier [15]. Thus, the arbitrary shaped barrier can be divided in a sum of small rectangular barrier. The total transmission probability is then the product of each rectangular barrier probability. For infinitesimally small barrier thickness, the probability expression can be expressed in integral form (2.3). The WKB approximation is a robust method whose the exactitude of the solution depends on the imaginary wave vector definition.

$$T \propto \exp\left(-2\int_{x1}^{x2} \mathrm{Im}(k_x)dx \right) \tag{2.3}$$

From air or vacuum barrier, the concept was extended to solid materials as for insulators and semiconductors. In solid materials, tunneling was first proposed by Zener to describe the breakdown of an insulator under strong electric field [16]. Later, the breakdown current of reverse biased p-n junction was interpreted as Zener tunneling process [17]. Under low forward bias, a tunneling current in heavily doped germanium p-n junctions was identified by Esaki [18]. Since then, different quantum and semi-classical models were developed to describe and quantify the tunneling transport.

2.3. Tunneling mechanisms in semiconductors

Theory of tunneling applied to semiconductors p-n junction is known as interband or band to band tunneling where the electron tunnels from the occupied states of the valence band to unoccupied states of the conduction band through a bridge in the imaginary k space that connect the two bands. As explained by Kane [1], the interband tunneling occurs over two mechanisms, direct and indirect tunneling (phonon assisted) (fig. 2.2).

According to Kane, direct tunneling occurs mainly in direct bandgap materials like InAs where bands extrema are located at the same point of the k space. The electron transition is made at the stationary phase point called branch point. Denoted k_B, this point is located in

the imaginary plan that connects the bands (fig 2.2). Direct tunneling is considered as an elastic process which implies the conservation of energy and perpendicular momentum.

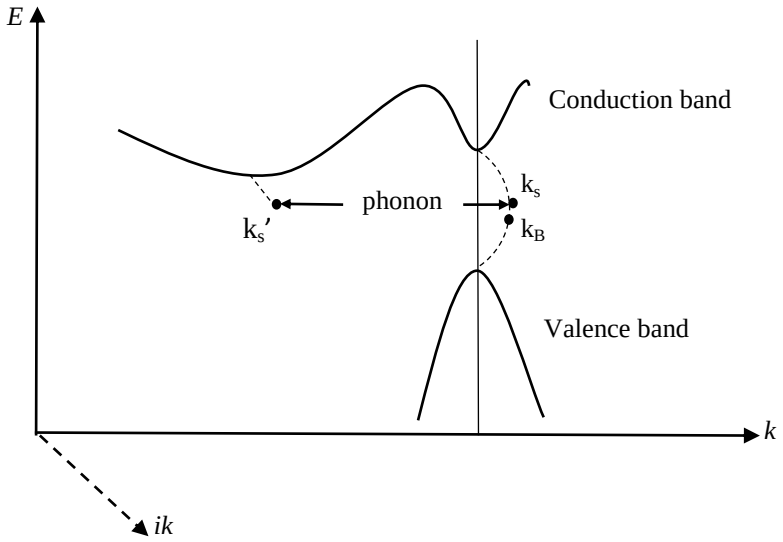

Figure 2.2 – Kane's illustration of the direct and indirect tunneling.

In indirect bandgap materials like Si or Ge where the conductance band minimum isn't located in Γ valley, tunneling is essentially indirect since the direct gap at k=0 is much larger than the indirect gap. However, the momentum offset due to crystal momentum difference between extrema involves phonons scattering to respect the momentum conservation condition. In this process, the electron transits from valence band maximum to a first point of stationary phase k_s in the same perpendicular vector, then scattering to a next point of stationary phase k_s' referring to conductance band minimum takes over resulting in phonon emission or absorption depending on bias polarity.

Another tunneling mode that combines different mechanisms is the trap assisted or impurity assisted tunneling (TAT) [19]. The TAT can either be elastic, or phonons assisted. In the presence of defects and impurities states located into the bandgap, tunneling is allowed from states of the same energy in a first time. The trapped carriers are then emitted by thermionic emission to the next region. Furthermore, the carrier emission is enhanced by phonon assisted tunneling in presence of external electric field. Moreover, if the bulk is

degenerately doped, the created band tail leads to further increase of the tunneling current. Overall, the excess current yielded by the TAT is considered as an undesirable leakage current.

Semiclassical tunneling models

More generally, theories beyond semiclassical models may be classified into two groups [20]. The first theory group treats tunneling inside the bandgap by assuming that through the Brillouin zone, electrons cycle repeatedly under a constant and modestly high electric field (stationary state), the tunneling occurs then between two eigenstates of same energy located at the bands edges. This theory group is currently designated by local tunneling by the fact that these models are spatially independent. In the second theory, tunneling is treated from outside the forbidden region according to scattering theory formalism. Tunneling probability is therefore derived from the probability densities ratio of the transmitted to the incident eigenstates represented by Bloch waves in respective bands. Contrary to the local tunneling, this theory group treats the tunneling as spatially dependent and is designated by nonlocal tunneling.

The most known of the local tunneling theory group is the Kane model. In his work, Kane decomposed the position operator x of the time independent Schrödinger equation into an intraband operator $i\hbar d/dk_x$ and an interband one. The interband transition is then removed by the introduction of a perturbation transformation. The interband transition is reintroduced via new matrix elements that link the different bands eigenstates of same energy. The tunneling probability is then integrated over the tunneling path. For local models, the turning points are replaced by the energy levels in the respective bands via a dispersion relation in the k-space. Kane used a two-band Hamiltonian to derive the energies expressions [6]. Therefore, a tunneling generation rate expression is derived from the maximum contribution to the tunneling probability located at the branch point which gives the locality aspect of the model. In a semiconductor of bandgap E_g and in the presence of a constant electric field F, the tunneling generation is expressed as:

$$G = \frac{F^2 m_r^{1/2}}{18\pi\hbar^2 E_g^{1/2}} \exp\left(\frac{-\pi m_r^{1/2} E_g^{3/2}}{2\hbar F}\right) = A_k F^2 \exp\left(\frac{-B_k}{F}\right) \qquad (2.4)$$

where m_r represents the reduced mass. Therefore, using the continuity equation, the tunneling current density can be evaluated by the integration of the generated electron density for each energy level with the associated local electric field:

$$J = -e\int G(x)dx \qquad (2.5)$$

Normally, the forbidden tunneling paths are associated with a low electric field and yields negligible generation rates. However, because of the internal electric field of the p-n junction, the previous generation rate expression presents the issue of a non-zero tunneling current in the absence of external electric field which is physically nonsense. In his next paper, Kane introduced the Fermi occupancy difference between the conduction and valence band of diode junction. The solution of the density of states as a function of the applied voltage reflects the Zener diode in reverse bias (i.e. generation) and the Esaki diode (i.e. recombination) in small forward bias.

Furthermore, Kane introduced the indirect tunneling that can be simply evaluated by setting the exponent of the electric field to 5/2. The Kane model was the basis of many other local models. In addition to band to band tunneling, Hurkx included the trap assisted tunneling as a separated recombination rate based on the SRH model [21]. Soon after, Schenk developed a simplified band to band tunneling model for silicon which demonstrated that the phonon assisted tunneling is predominant under all circumstances. His rigorous theory includes the electron-phonon collision in the perturbation operator and takes into account the anisotropy of the six conduction band valleys. For direct semiconductors, bands parabolicity and isotropy in the vicinity of k=0, i.e. the minimum bandgap, is considered. Instead of the transmission probability, the model was developed basing on the differential tunneling conductivity. The current is then obtained by integrating the conductivity over the tunneling path. More importantly, the Schenk model permits to evaluate the tunneling current under strong and inhomogeneous electric field which is more realistic in the case of tunnel transistors. The simplified model for numerical tools, in a form of a generation rate expression, makes use of the Kane's two-band model and implies critical field strengths. Also, the tunneling rate expression includes the Fermi function that describes the tunneling generation, recombination and zero applied voltage [22].

Tunneling in confined systems was recently treated in a simple manner of bandgap scaling (BGS) [23]. The modified bandgap $E_{g,QC}$ due to 1-D and 2-D quantum confinement (i.e. quantum well and nanowire) and the resulting reduced mass variation are used to reevaluate the Kane generation rate parameters. Using the k.p method, the confinement effect on the imaginary dispersion relation analysis shows that the conduction band and the light holes valence band effective masses are sufficient to evaluate the tunneling current. Therefore, expressions of the prefactor A_k corresponding to lower dimensions were derived as follows:

$$A_{2-D} = \frac{q\sqrt{m_r E_{g,QC}}}{18\hbar^2}\left[\sqrt{\frac{q\pi F}{4B_{BGS}}} + 0.185\left(\frac{qF}{B_{BGS}}\right)\right] \tag{2.6a}$$

$$A_{1-D} = \frac{2q\pi^2}{9h} \tag{2.6b}$$

$$B_{BGS} = B_{bulk}\left(\frac{E_{g,QC}}{E_g}\right)^2 \tag{2.6c}$$

$$m_{r,QC} = m_r \frac{E_{g,QC}}{E_g} \tag{2.6d}$$

Non-local model

If the constant electric field assumption is commonly accepted for p-n junctions, it is hardly applicable for other devices. Indeed, the exponential dependence of the generation rate on the electric field implies that a small variation of the latter yields large current overestimation. Therefore, non-local models that take into account the exact potential barrier produce a more accurate tunneling estimation. As aforementioned, the non-local models evaluates the tunneling generation in spatial coordinate. The tunneling probability for a given energy E_1 is evaluated by the integration of the imaginary k vector over the transition path limited by the turning points x_1 and x_2 (2.3) as illustrated in fig. 2.3. The tunneling current density can then be obtained by integrating the tunneling probability over all the possible paths of the tunneling window, i.e. the available energy states comprised between the respective regions valence and conduction bands. The current density

expression that combines the WKB approximation with the Landauer's conduction formula has the general form [24]:

$$J = \frac{e}{\pi\hbar Area}\int\sum_{k_\perp} T\left(E,k_\perp\right)\left[f_v\left(E\right)-f_c\left(E\right)\right]dE \qquad (2.7)$$

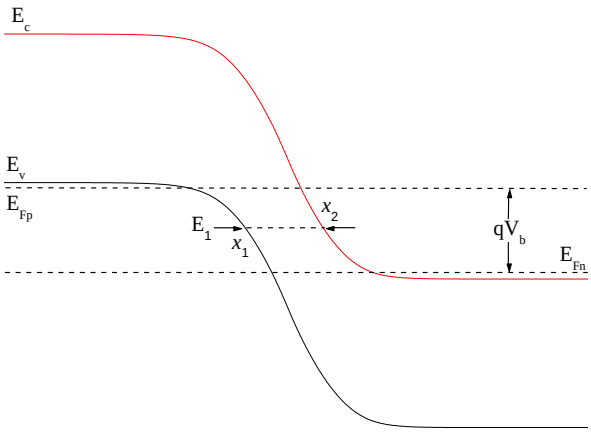

Figure 2.3 – Reverse biased p^+-n^+ junction band diagram illustrating a possible tunneling path of energy E_1 and the corresponding turning points.

The non-local approach differentiates the generation rates for electrons and holes, unlike local model where identical rates are obtained. It is noticed that both local and non-local approaches treat the tunneling as a one dimension phenomenon. Thus, for numerical simulation purpose, the most probable tunneling path axis has to be chosen beforehand. If this assumption is valid for p-n junctions, the case is more delicate for tunnel transistors where the perpendicular electric field add up to the parallel component and yields 2-D tunneling trajectory as revealed by simulations [25]. Also, the tunneling direction changes with the gate bias variation, complicating the choice of the right path direction. Therefore, an underestimation of the tunneling current might result.

Overall, non-local models yield more precise solutions and are easily evaluated in numerical simulation tools. However, the use of such expressions might be difficult for analytical modeling purpose. The direct mathematical integration being impossible to perform, some assumptions must be introduced in order to obtain an explicit tunneling current expression.

Generally, the Fermi occupancy factors difference is assumed to equal 1 for a sufficient applied voltage that ensures the total opening of the tunneling window, and 0 in the other case. The simplification that has a major impact on the probability evaluation is the barrier profile assumption. In fact, arbitrary shaped profile with a known solution has to be used. The most common profile is the triangular barrier which is equivalent to the constant electric field assumption [12]. This approach yields the same results as the Kane model with the same overestimation issue (the demonstration of the Kane generation expression can be obtained with the non-local model using the previous enumerated assumptions [26]). On the other hand, the exponential shape is more accurate (as in gated p-i-n junctions). Unfortunately, the derived expression of the tunneling probability cannot be analytically integrated. As a result, numerical integration methods must be used [27].

2.4. Tunnel field effect transistor

The idea of exploiting tunnel phenomenon in transistors is almost old as tunneling theorization. The first tunneling based transistor was proposed by Chang and Esaki in 1977 [28]. Their p-n-p triode used heterojunctions to create tunneling conditions and the current flow was modulated by the base bias. However, for next decade, researches were mainly focused on resonant tunneling diodes (RTD) and its negative differential resistance behavior (NDR). We had to wait until 1988 to see the fabrication and the characterization of the first Si-based TFET [29].

In 1992, a heterojunction p-i-n TFET was successfully fabricated [30]. Nevertheless, no particular interest was made on TFETs since the exhibited characteristics were not advantageous compared to MOSFET even with the apparition of major degradations due to downscaling. The real infatuation for TFETs came with the fabrication of the first steep subthreshold slope TFET [7]. Based on carbon nanotube (fig 2.4), this TFET achieved a 40 mV/dec SS; however, it steel suffered from low on-current. The race for TFET optimizing was launched.

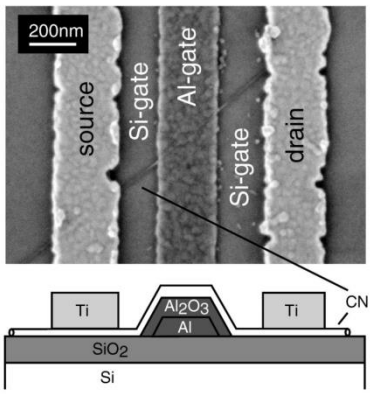

Figure 2.4 – SEM and cross sectional view of the carbon nanotube TFET (CNT TFET) structure fabricated by IBM [7].

2.4.1. Working principle

Let's now interest on the working principle of tunnel field effect transistor. Fig 2.5 illustrates the corresponding band diagram for different states of a basic TFET. This latter has a similar structure to the conventional MOSFET, except that the source is filled with p-type dopant which makes it look as a gated p-i-n diode. The tunneling junctions are then created by the difference between the channel and extensions built in potential.

First, we have to keep in mind that the band to band tunneling occurs between two bands extrema of the same energy level (energy conservation condition). In the off-state, the conduction band of the channel is set to a higher energy than the source valence band (fig 2.5a). No state is therefore available for band to band tunneling. Ideally, no current flows in the device. However, an off-state current is observed. Indeed, diverse leakage mechanisms contribute to raise this off-current [12]. The temperature dependency of the off-current highlighted by measurements suggests the presence of traps at the source and drain junctions resulting in a TAT. Also, as in a p-n junction, the Shockley–Read–Hall carrier generation arises from the source and drain depletion regions. For channel length less than 20 nm, direct and TAT from the source to the drain become dominant. Moreover, if the drain extension is sufficiently doped, a tunneling junction is created and electrons flow from the channel valence band to the drain conduction band. The drain current depicts then an ambipolar behavior and results in the increase of the minimum current (fig 2.5d). As in MOSFETs, carriers might tunnel over the oxide layer between the channel and the gate

providing an important leakage current. Either for metallic or poly-silicon gates, direct, trap-assisted, and Fowler-Nordheim tunneling mechanisms can be involved [31].

As V_{gs} increases (fig 2.5b), the channel conduction band gets lower until it aligns with the source valance band level producing the tunneling onset. In theory, neglecting all the leakage mechanisms, the opening of the tunneling window for few gate millivolts associated with the exponential tunneling probability increase produce the ideal steep subthreshold slope. The continuous channel bands lowering yields an enlargement of the tunneling window. Simultaneously, the bands lowering causes a relative thinning of the barrier. In consequence, the tunneling current rises exponentially according to tunneling probability formula. As aforementioned, the electric field over the TFET junctions is not constant. Accordingly, the carries tunnel over multiple paths of different distances with distinct tunneling probabilities. The TFET is now turned on and the tunneling barrier is modulated by the gate (fig 2.5d). Furthermore, if the TAT can be involved for lower gate voltages, the direct band to band tunneling takes advantage while the tunneling window is totally open. On the other hand, the bands lowering reduces the overlap of the channel valance band over the drain conduction band. The ambipolar current decreases till the disappearance of the overlap, the drain tunneling junction is now turned off.

When the gate bias is further increased (fig 2.5c), the channel potential saturates so it slightly exceeds the drain potential. The electron density in the channel reaches the drain doping level. The inversion layer is then pinned to the drain and the tunneling barrier is now modulated by the latter. Even if the bands overlap remains practically unchanged, the tunneling current still increases. Indeed, although the strong inversion layer is pinned to the drain, the gradient density near the source enhances leading to a more abrupt band bending and hence a thinner barrier. Let's consider the output characteristic depicted in fig 2.5h. For a given gate bias, a tunneling junction is created in the source side. In the absence of a drain supply, the null difference between the source and drain Fermi levels results in null drain current. As V_{gs} remains constant, the tunneling barrier is rather modulated by the drain. The channel potential is then pinned to the drain by means of the electron's quasi Fermi level. The channel bands lower linearly with V_{ds} increase yielding an enlargement of the tunneling window and a thinning of the barrier.

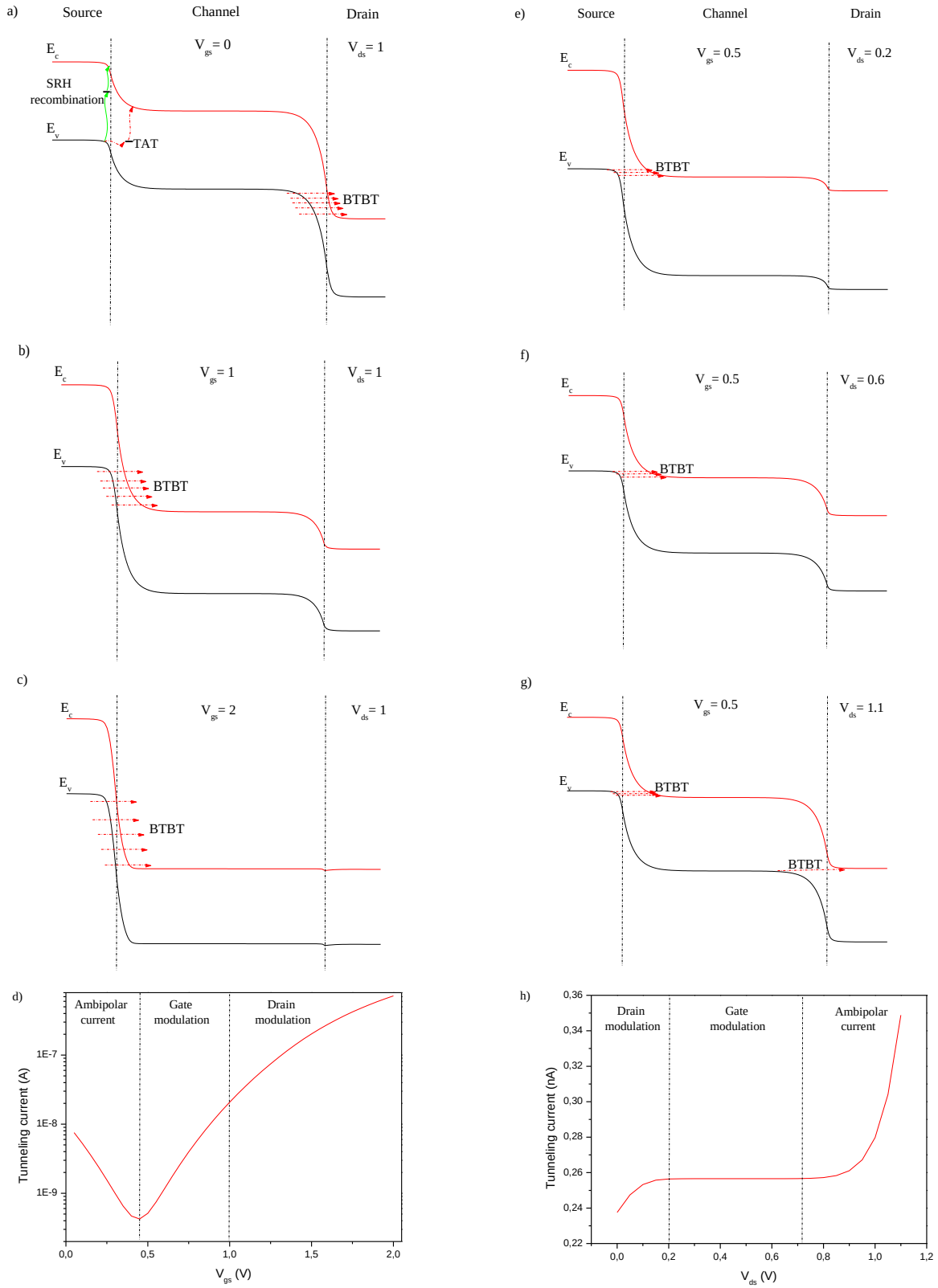

Figure 2.5 – (a,b,c) band diagram of undoped n-TFET for different applied V_{gs} and (e,f,g) different V_{ds}, (d) the transfer characteristic, (h) output characteristic illustrating the different conduction regimes.

The tunneling current increases quasi-linearly which is analogous to the ohmic region in MOSFET's output characteristic (fig 2.5e). The pinning of the channel to the drain decreases as well and the electrostatic control of the gate over the channel is restituted. The tunneling barrier remains then unchanged producing saturation-like of the drain current (fig 2.5f). The ambipolarity behavior appears also in the output characteristic (fig 2.5g). Unlike in MOSFETs where high drain bias yields kink effect and breakdown of the current, TFETs exhibit an ambipolar current due to the creation of tunneling junction in the drain side.

2.4.2. TFET characteristics and metrics

The most interesting TFET characteristic is its theoretical steep subthreshold slope. Although the subthreshold concept is less intuitive in TFETs, the subthreshold slope is broadly used as a key performance. As explained in the first chapter, the MOSFET's subthreshold slope is approximately constant over the weak inversion regime and has a weak dependence on V_{gs}. In TFETs however, the subthreshold slope is strongly dependent on V_{gs}, it can be expressed as [32]:

$$SS_{TFET} = \frac{V_{gs}^2}{5.75(V_{gs} + Const)} \tag{2.7}$$

where the constant value depends on the device dimensions and material parameters. This particularity of the SS in TFETs leads to the introduction of a new metric. In addition to the minimum slope called also point slope that is used as a proof of the tunneling efficiency, the average slope traduces the switching performance over the entire subthreshold regime and is more used for benchmarking than the point slope. The SS_{avr} is extracted over the subthreshold regime defined from the off-state gate voltage to the threshold voltage as:

$$SS_{avg} = \frac{V_{th} - V_{off}}{\log_{10}(I_{ds}(V_{th}) / I_{ds}(V_{off}))} \tag{2.8}$$

If in MOSFETs, the threshold voltage is physically defined as the transition from weak to strong inversion regime. There is no consensus on the extraction method in TFETs. Indeed, the transport and switching mechanisms being totally different, the classical MOSFETs threshold voltage definition fails to give an equivalent physical insight in TFETs.

Nevertheless, the constant current method which is the most popular definition is generally used. The first physical definition of the threshold voltage in TFETs was proposed by Boucart and Ionescu [33] as the saturation point of the barrier width narrowing (i.e. the transition between the quasi-exponential and linear dependence of the current on the gate bias). This definition corresponds to transconductance change (TC) method, which is also valid for MOSFET and defined as the voltage corresponding to a null second derivative of the transconductance. A comparative study based on simulations between their definition and the constant current method was carried out. It was shown that the arbitrary constant current value (10^{-7} A/µm) doesn't depict any physics or mechanism involved in the tunneling current. This technique provides also lower threshold values compared to the TC method. On the other hand, the TC method has a weak dependence on the gate length. Accordingly, it cannot properly reflect the threshold voltage roll-off and the drain induced barrier thinning (DIBT).

The I_{on}, I_{off} and their ratio are also important metrics for device benchmarking. In order to be competitive to CMOS, it is important to align TFETs metrics to those of low power MOSFET. As a reference for LP CMOS, the approximate targeted values are I_{on} = 1567 µA/µm, I_{off} = 100 pA/µm and V_{dd} = 0.75 V [34].

If a higher on-current is required, the gate modulation must be prolonged so that a thinner tunneling barrier and a larger tunneling window are attained. This can be achieved by increasing the drain voltage (fig 2.6a). In this way, the pinning of the channel potential to the drain is delayed to higher gate biases (fig 2.6b). Nevertheless, increasing the drain supply has also an impact on the drain tunneling junction leading to a thinner barrier and a larger band offset. In consequence, the ambipolar currents as well as the off-current are enhanced. The current minimum moves forward with V_{gs} and the subthreshold slope is degraded.

As In MOSFETs, the saturation in TFETs occurs when the channel is decoupled from the drain. However, the physics beyond this decoupling is different. The saturation in MOSFETs is a consequence of the extension of the depletion region under high electric field, yielding a pinch-off of the inversion layer near the drain junction. Whereas in TFETs, The saturation occurs when the barrier modulation switches form the drain to the gate terminal.

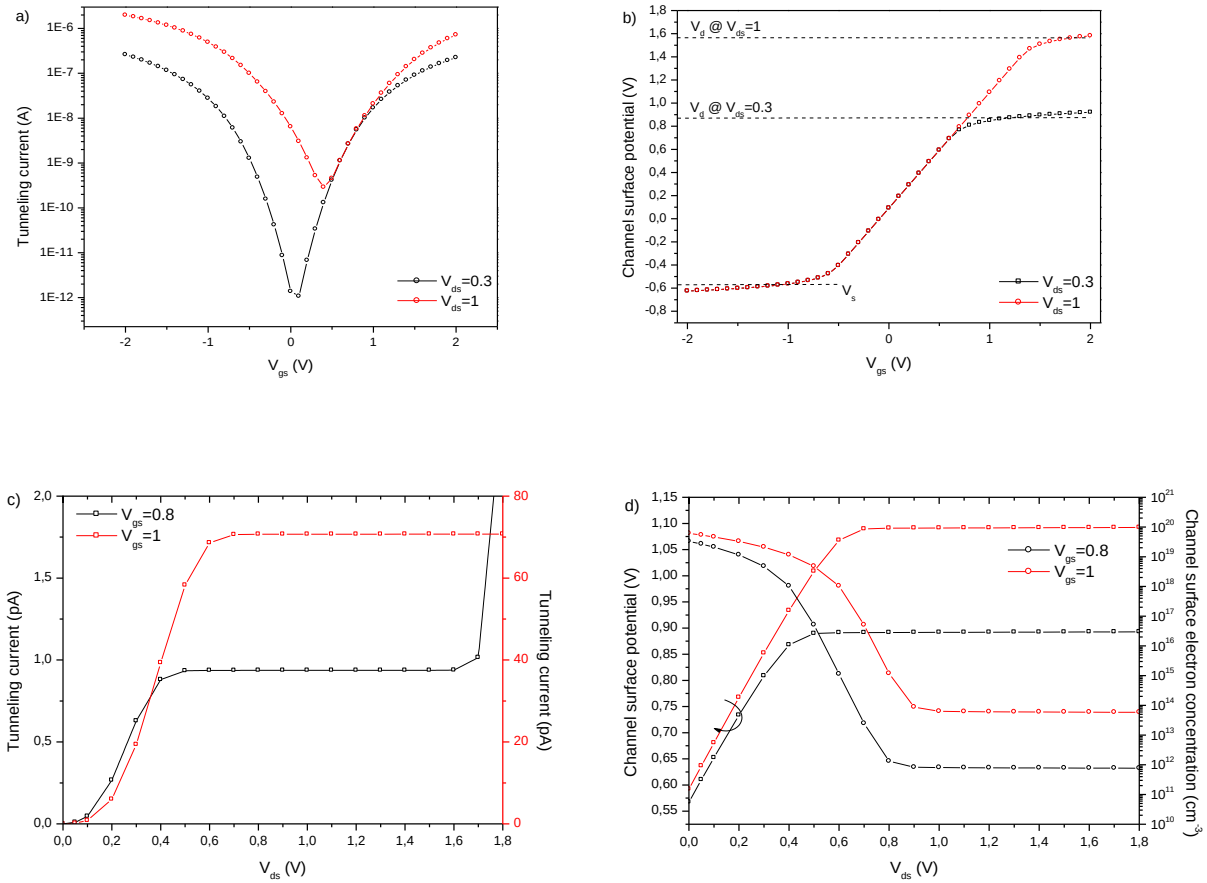

Figure 2.6 – Symmetric TFET (a) transfer characteristic, (b) corresponding channel surface potential, (c) output characteristic and (d) corresponding channel surface potential and surface electron concentration for different biases.

The good saturation of TFETs provides a very low output conductance which is ideal for some analog/RF applications. For instance, TFETs can be suitable for common-source amplifiers where high gain and high output impedance are needed. However, a strong dependence of V_{dsat} on V_{gs} is observed, depicted by what is known as the delayed saturation (fig 2.6c). This effect results from the fact that higher drain supply is needed to pull down the channel barrier respectively to the drain, which ensures a decrease of the pinning and drains the inversion layer carriers (fig 2.6d). The delayed saturation represents a serious inconvenient. In digital applications, this feature leads to noise margin degradation and power consumption enhancement.

Furthermore, TFET suffers from high gate to drain capacitance that enhances the Miller effect. This enhanced capacitance is principally due to the channel inversion layer while the gate to source capacitance results from the depletion charge [35]. It is worth noting that the majority of the inversion carriers arises from the thermionic emission over the drain built-in potential while the tunneling process has a minor impact on the layer formation [36]. Thus, an increasing of the inversion layer by a lowering of the drain barrier (lower V_{ds}) leads to an enhancement of the Miller capacitance as depicted in fig 2.7. This effect constitutes a major limitation for ultra-low power applications. Furthermore, the transient analysis of TFET based inverter shows high overshoot/undershoot peaks in the output voltage. In addition, the enhanced capacitance yields higher propagation delay [37]. In consequence, the total power consumption is increased which represents a drawback for low power digital applications.

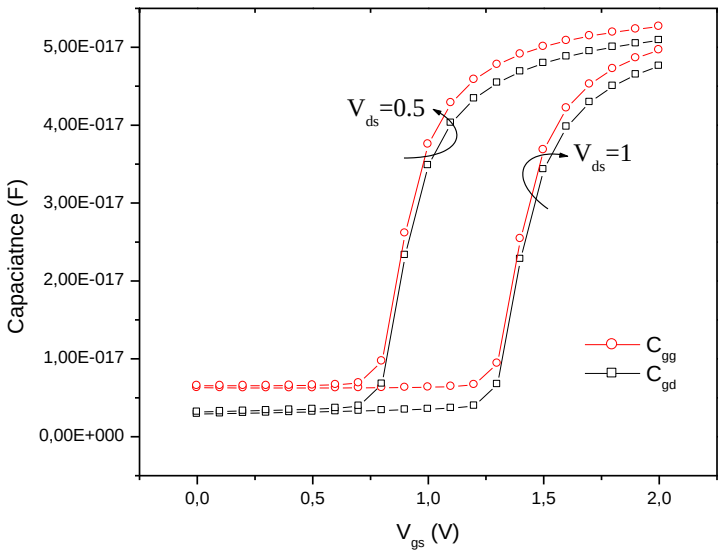

Figure 2.7 – C_{gg} and C_{gd} as function of V_{gs} of a symmetric undoped TFET for V_{ds}=0.5, 1 V.

2.4.3. Transport mechanisms in TFET

If electrons flow from the source to the channel via tunneling process, the transport of the generated carriers over the remaining channel distance to the drain is governed by drift-diffusion transport (DD). Intuitively, TFET can be seen as an ideal gated tunnel diode coupled in series with an ideal MOSFET via an internal node (fig 2.8) [38-39]. Consequently, DD transport can be considered as a limiter of tunneling current.

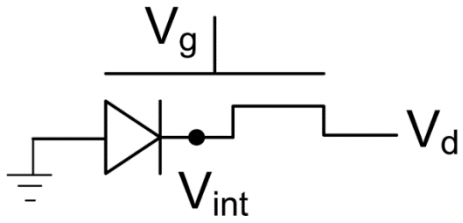

Figure 2.8 – Physical representation of the coupled tunneling and drift-diffusion transport modes.

In [39], an interesting demonstration of the effect of coupled transport modes on the tunneling current limitation was performed. For this purpose, the tunneling current was evaluated via the resolution of the Poisson equation with no continuity equation resolving. The current was then calculated by integration of the tunneling generation rate over the volume. It appears that the DD limitation occurs approximately above 10 µA/µm and takes importance with current increasing. Below this limit, the current is tunneling limited which means that all the generated carriers flow through the channel with no limitation. Otherwise, the author proposed another manner of extracting tunneling limited current by setting mobility to infinity and null velocity saturation, we followed this procedure to extract the coupled transport effect in VSG TFET as illustrated in fig 2.9 (the mobility was intentionally decreased in order of 10 cm^2/Vs in the full transport mode to amplify the attenuation effect). In this way, it is possible to evaluate the impact of DD transport as an attenuation factor as shown in fig 2.9; the full transport current can then be expressed as $I_{ds} = f(I_T) I_T(V_{gs}, V_{ds})$ [39].

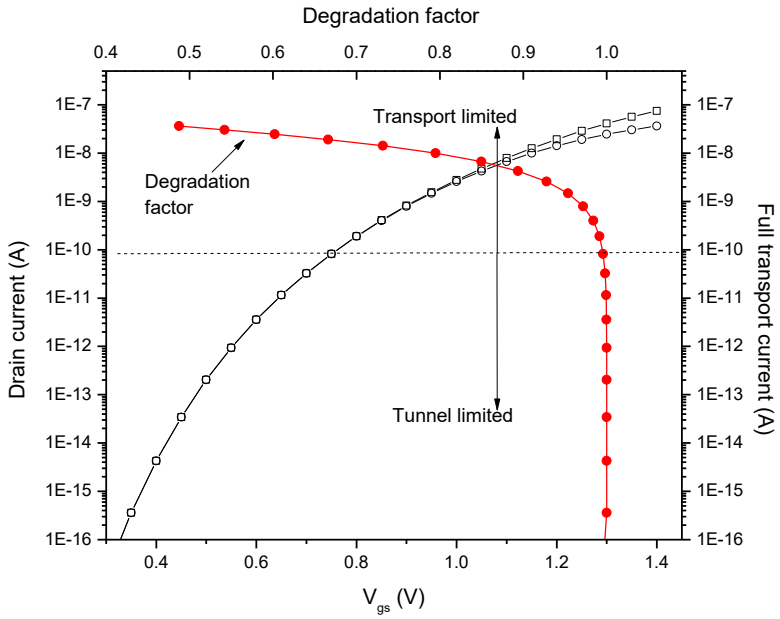

Figure 2.9 – Transfer characteristic of a VSG TFET showing the impact of full transport mode on the limitation of tunneling currant, and the corresponding full transport degradation factor.

2.4.4. Different TFET configurations

In addition to some characteristic similarities between TFET and MOSFET, the tunneling transistor can take any known architecture, double gate, surrounding gate, planar, pillar, vertical, nanowire and so on. The only condition is the creation of tunneling junction and the possibility of its modulation. Upon the tunneling path, TFETs can be classified into two main types. The most common one is known as point-TFET referring to the junction point of the source and channel at the oxide interface aligned with gate edge. It is noticed that the main contributing tunneling to the total current occurs at this junction point in parallel to the gate (fig 2.10a, b). This TFET type exhibit a scaling capability similar to MOSFETs. Nevertheless, due to the small tunneling volume, point-TFET suffers from low on-current. Moreover, the high gradient source doping in addition with the precise alignment of tunnel junction with the gate edge represent a technical challenge. If the gate is underlapped, the electrostatic control over the junction is degraded and sub 60 mV/dec SS becomes unreachable.

Conversely, if the gate overlaps the source, field induced carrier depletion might occur. Hence, the tunneling injection from the source is decreased [12].

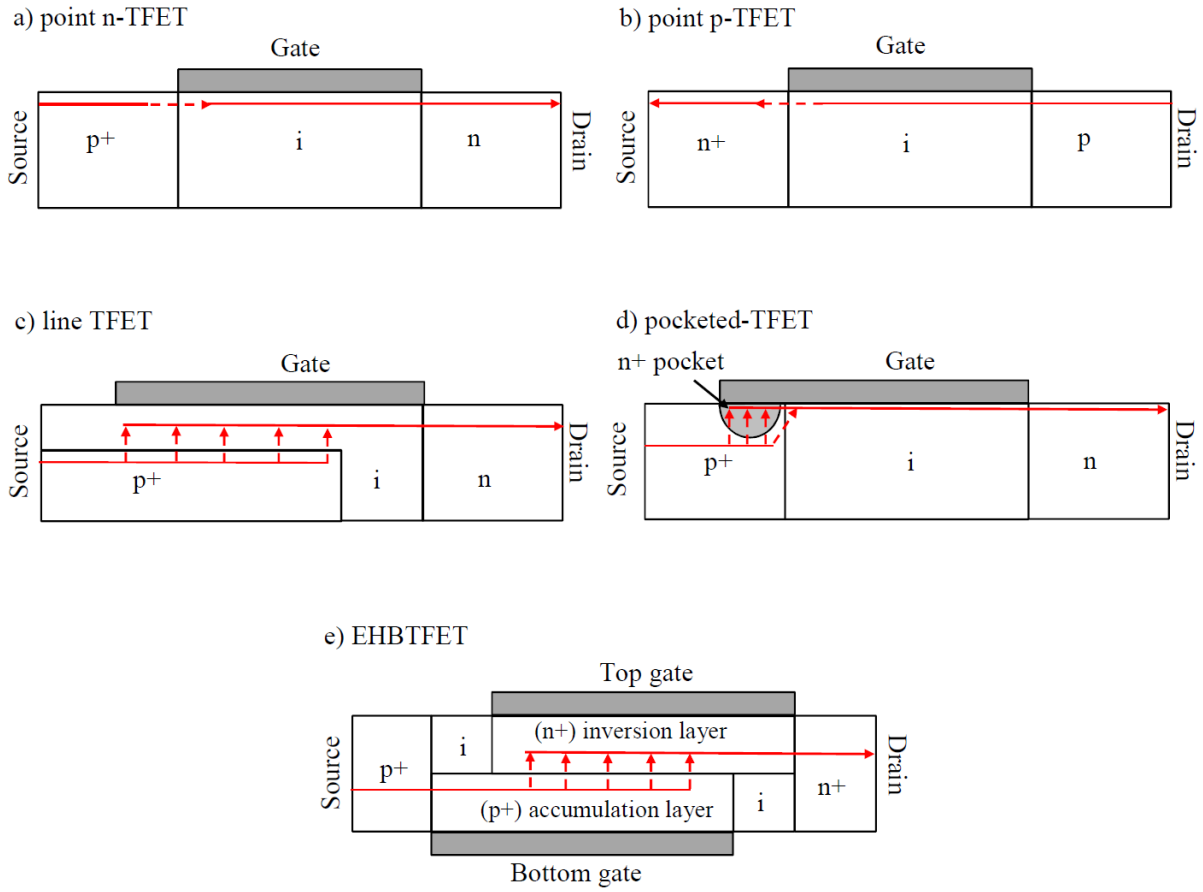

Figure 2.10 – Different TFET configurations. The full red arrows indicate the drift diffusion carrier flow, the dashed arrows indicate tunnel paths.

For the second type called line-TFET, the tunneling path is perpendicular to the gate. In this configuration, the gate is disposed on the source extension resulting on multiple tunneling paths of high generation rate (fig 2.10c). Thus, a much higher on-current and a steeper slope are expected in line-TFETs compared with point-TFET. Indeed, it was shown that the electron-hole bilayer TFETs (EHBTFET) which is a line-TFET type structure can achieve a 10 mV/dec SS (fig 2.10e) [40]. In practice however, line-TFETs like pocketed TFETs (fig 2.10d) are complex to realize as they are very sensitive to the doping profile and concentration

[41]. Since the channel must be as thin as possible in order to have a better control, the quantum mechanical effects such as size and field induced quantization must be taken into account [26]. Another issue of the line-TFETs structures is the direct dependence of tunneling current on the gate length which limits seriously the scaling capability.

2.5. TFET enhancement

In addition to a low on-current, TFETs rarely achieve a sub 60mV/dec SS in practice, especially for silicon body. TFETs are also characterized by low transconductance and cutoff frequency relatively to MOSFETs. In sum, many drawbacks that put in question TFET's reliability as a potential solution for future low power applications. Considering a triangular barrier shape in a p-n junction, the integration of (2.3) using the WKB approximation gives the following tunneling probability expression [12]:

$$T_{WKB}^{3D} = \exp\left(-\frac{4\sqrt{2m_r}\left(E_g + E_\perp\right)^{3/2}}{3q\hbar F} \right) \tag{2.8}$$

where $E_\perp$ represents the transverse energy component of the total energy. From this equation, it appears that to enhance tunneling probability, one may choose material with low reduced effective mass or equivalently narrow bandgap. Another way would be to increase the electric field. If an exponential tunneling barrier is considered, the maximum electric field at the junction will be:

$$\left|F\right| = \left|\frac{V_c - V_s}{\lambda}\right| \tag{2.9}$$

where V_c and V_s are respectively the channel and source junction voltage, λ represents the scaling length. Thus, it is possible to improve the electric field by increasing the source built-in potential (i.e. increasing the p-type doping yielding higher negative potential) or by reducing the scaling length via the structure type and dimensions variation. Therefore, various solutions can be explored to overcome TFETs' limits. Geometry, material, gate and doping engineering reveal as suitable for TFET enhancing.

2.5.1. Geometry dependence

Besides improving the electrostatic control over the channel, multigates improve as well the control of the tunneling barrier by reducing the tunneling screening length as illustrated in fig 2.11-12 [10, 12, 42]. As for MOSFETs, the surrounding gate appears to be the most efficient structure since it has the lowest characteristic length compared to other multigates [12]. Furthermore, the inverse proportionality of the characteristic length to the channel thickness suggests that the reduction of this latter improves the device control over the tunneling barrier. Experiments show that in addition to the tunneling current enhancement, the channel thinning improves the transconductance as well (fig 2.11). Moreover, the NW structure with reduced radius yields a remarkable improvement of the output conductance and the intrinsic gain [10].

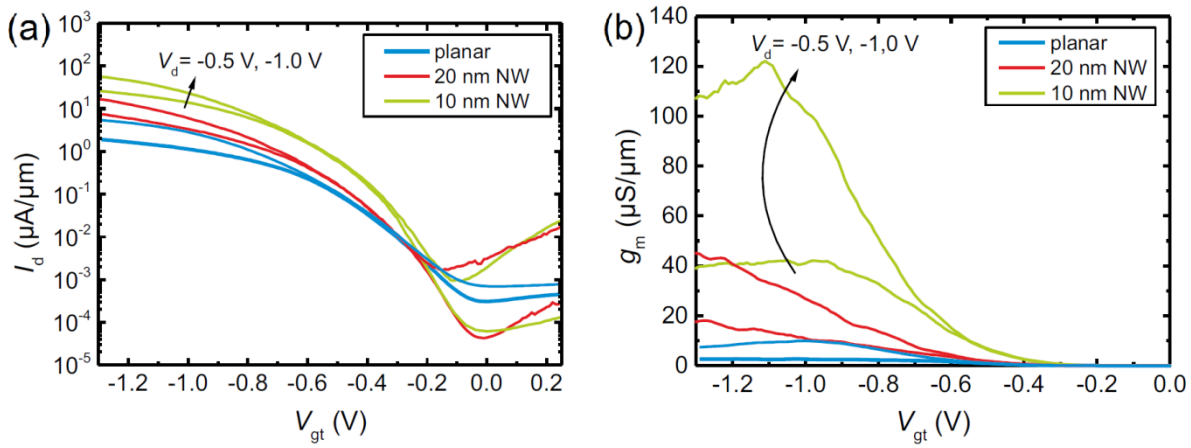

Figure 2.11 – Experimental (a) Transfer characteristic and (b) transconductance illustrating the improvement of GAA NW compared to planar p-type TFET [10].

However, for ultrathin bodies, the quantum confinement becomes important leading to an enhancement of the effective mass [42]. Consequently, the tunneling probability decreases. The 2-D size-induced quantum confinement in nanowires is so significant that it screens the electrostatic control efficiency of the structure. As depicted in the next figure, if the GAA is the most efficient structure for larger channels, the DG takes the advantage for ultra-thin bodies.

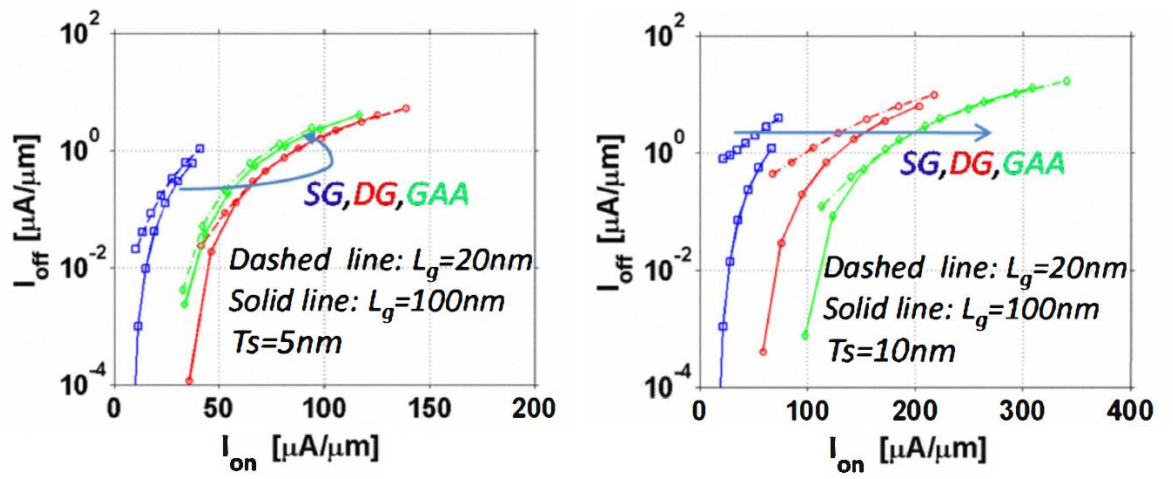

Figure 2.12 – Relation between the off and on-current for InAs based SG, DG, and GAA TFETs for L_g=20, 100 nm, T_s=5 nm (left panel) and T_s=10 nm (right panel) [42].

Although TFETs exhibit a better immunity against SCEs than MOSFETs, this feature is significantly degraded for sub 30 nm channel lengths [43]. The above figures depict an increase off-current for ultra-short channels, yielded by the enhancement of different leakage mechanisms with dominant direct tunneling form the source to the drain. In analogy with the DIBL in MOSFETs, the drain induced barrier thinning (DIBT) is an important figure of merit. The DIBT gives a general overview of the drain bias impact on the tunneling barrier modulation. For long channels, the gate modulation of the barrier is totally independent of the drain; the DIBT is then quasi null. For ultra-short channels however, the DIBT increases exponentially with respect to length reduction, traducing an enhancement of the drain voltage control on the tunneling barrier during gate modulation as shown in fig 2.13. Studies demonstrate also that the DIBT is significantly reduced with the thickness reduction, especially for ultra-short channels [42, 43, 44].

The reduction of the gate oxide thickness is another way of enhancing the tunneling current, device controllability and resilience to SCEs [43, 44]. However, due to the increasing gate leakage current, large bandgap dielectrics like high-κ materials must be used as a replacement of the silicon oxide or as a stack of the two materials. The High-κ dielectric has also an important impact on the threshold voltage as it positively shifts with the permittivity increase [44]. This variability can be useful in the reduction of the power consumption and

the alignment of the operating voltage in mixed CMOS-TFET conceptions. Also, it is noticed that the device performances still improve with the increasing of the high-κ values even if the effective oxide thickness is kept the same [44].

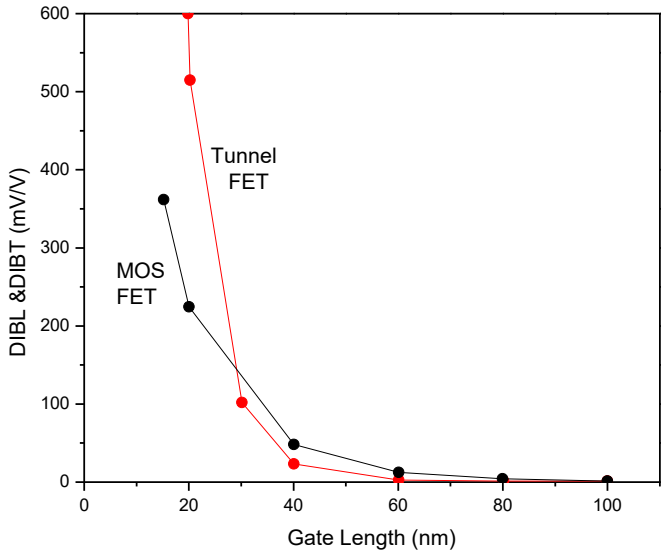

Figure 2.13 – DIBL (MOSFET) and DIBT (TFET) for homojunction $In_{0.53}Ga_{0.47}As$ double-gate MOSFET and TFET with T_s=10 nm, T_{ox}=6 nm, and ε_{ox}=9 [43].

2.5.2. Gate engineering

Another solution for threshold voltage shifting is to vary the gate workfunction. In fact, increasing the workfunction can be interpreted as a gate voltage lowering. Thus, the channel potential drops leading to a relative reduction of the tunneling barrier. If we consider the transfer characteristic, it appears to shift to the right. The threshold voltage is shifted into the same direction. Otherwise, workfunction engineering has a minor impact on the global device response [45]. Among the devices that exploit this feature, dual workfunction gate based TFET can be an interesting configuration. By setting an auxiliary gate near the drain side with a higher workfunction, the gate modulation of the drain tunneling barrier is shifted which is reflected by an attenuation of the ambipolar current. Furthermore, the auxiliary gate creates a barrier in the channel that blocks the current in the off-state resulting in a steeper subthreshold slope [46]. In another manner, the EHBTFET

exploits the workfunction difference between the top and the bottom gate to create the needed inversion and accumulation layers [40].

As aforementioned in TFET configurations, the gate overlapping on the source extension enhances the mixed point and line tunneling. On the other hand, the gate underlapping on the drain side decreases the gate modulation of the drain tunneling junction. As a result, the ambipolarity can be totally suppressed [46, 47]. With a reasonable underlap, the channel control can be conserved and the on-current can be maintained at its highest value. Moreover, simulations demonstrate a remarkable improvement of the analog/RF FOMs and a noticeable reduction of the gate to drain capacitance which is essentially due to the reduction of inversion layer area [47].

2.5.3. Material engineering

Electronic industry development was carried by the large availability and the low cost of silicon. The process simplicity of silicon based devices and the good properties of its native oxide made of the silicon as the material of choice over more than a half century. With the apparition of major degradations with downscaling, strained-Si allows to extend the viability of Si-based devices. The high mobility and injection velocity that characterize the Strained-Si lead to significant drive current and other parameters improvement [48]. In TFET, the low bandgap of strained-Si can be used to enhance the generation rate [49]. Nevertheless, if the strain is formed over the entire channel, the ambipolar current is increased as well. Hence, a lateral stain is more judicious. The aim of this latter is to form an asymmetrical strain profile which decays from its highest value at the source junction to a normal disposition at the drain junction. The tunneling form the channel to the drain is therefore maintained at its normal rate. In [49], the effect of various mechanical lateral strain profiles was explored. With a bandgap shrinkage peak of 0.2 eV, the lateral strain profile improves the current while keeping the ambipolar current at its lowest level (fig 2.14). Consequently, the point subthreshold slope is reduced around 12 mV/dec.

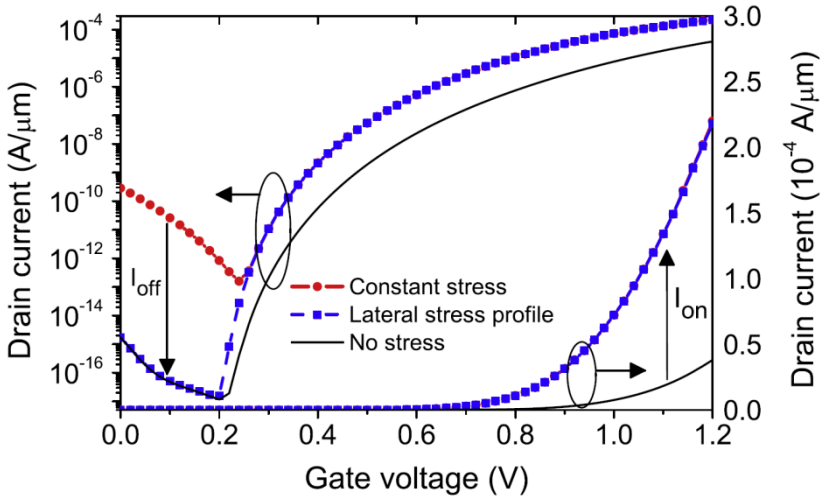

Figure 2.14 – Drain current versus gate voltage for all-silicon DG Tunnel FETs with and without strain profile (L_g=50 nm, V_{ds}=1 V) [49].

Thus, it appears that the most efficient way of tunneling enhancement is without contest the material engineering by acting directly on the bandgap. In this purpose, narrow bandgap and low effective-mass materials can be used. Studies demonstrate the potential of narrow bandgap materials like Ge and III-V compounds to provide higher on-current at lower bias than Si-based TFETs [42, 12, 50]. For Ge-based TFET, the on-current is boosted 2700 times for a p-type and 335 times for an n-type compared to equivalent Si-based TFET [50].

Over the past decade, researches have been intensified on the use of high mobility materials as current booster. In this research field, III-V semiconductor alloys are considered as promising materials due to their high mobility and low carrier effective mass. Moreover, the high injection velocity that characterizes such materials may be a solution for ultra-short channels issues in which the ballistic transport dominates and where the injection velocity becomes an important factor. Moreover, III-V compounds and alloys offer a large variety of direct and narrow bandgap semiconductors as InAs and InSb, which is ideal for tunneling efficiency enhancement. However, a lower bandgap leads to an increasing of the off-state current and a major degradation of the subthreshold slope. In addition to the ambipolar current enhancement, leakage mechanisms like the TAT and SRH generation enhance as well. Furthermore, the direct and defect assisted tunneling from the source to the drain in

ultra-short channels is aggravated [12]. Likewise, the field-induced and size-induced quantum confinement increases with the reduction of the carrier's effective masse [51].

The first III-V based TFET was realized in 2009 [52]. Using $In_{0.53}Ga_{0.47}As$ alloy in a 100 nm gate length vertical structure, this TFET was characterized with an I_{on} of 20 µA/µm, an I_{on}/I_{off} ratio of 10^4 and a SS_{min} of 190 mV/dec. The device was also characterized with high traps density at the Al_2O_3 interface which induced high and penalizing leakage current in addition to the SRH generation and TAT mechanisms. Thus, advances had to be made in order to reduce process induced defects and the interface trap density. In 2011, an $In_{0.53}Ga_{0.47}As$ based TFET of 77 mV/dec SS_{min} was successfully fabricated which was then the best performance for a homojunction TFET. In the same work, a 58 mV/dec SS_{min} heterojunction TFET was achieved using an $In_{0.7}Ga_{0.3}As$ pocket at the tunnel junction [53].

The tunneling efficiency in heterostructures is the result of a lower bandgap at the tunneling junction. This effective bandgap E_{geff} lower than those of both materials results from the band offset and the type of the heterojunction band alignment. This latter can be classified into three types, straddling, staggered and broken. A staggered type yields small positive E_{geff}, while a broken band alignment yields negative values. For instance, a 40 meV E_{geff} is obtained for $InAs/Al_{0.45}Ga_{0.55}Sb$, 0.2 eV for InAs/Si and 101 meV for s-Si/s-Ge on relaxed $Si_{0.48}Ge_{0.52}$.

Thus, a very thin tunneling junction can be created from the natural band alignment of the heterojunction. However, the electrostatic control of this tunneling junction must imperatively cover the total junction, especially for broken gap structures. Otherwise, an undesirable and uncontrolled tunneling will raise the off-current. This may require an additional gate supply to totally turn-off the tunneling junction. In practice, multigates structures are suitable for the majority of heterostructures.

Heterostructures involving different III-V materials and alloys pave the way to wide material engineering options. Indeed, narrow staggered or broken gap alignment and lattice matching become possible by modifying the compounds compositions and disposition. The effect of band alignment types and alloy composition on some TFET key performances was carried out in [54]. The next figure illustrates the optimal composition and band alignment that provides the best I_{on}, I_{off} and SS for a broken gap InAs/GaSb and staggered gap

InAs/AlSb heterojunctions. The best performances are obtained for a 60% Al molar fraction yielding 0.094 eV effective bandgap. In addition, the results show an efficient source doping of 10^{19} cm^{-3}.

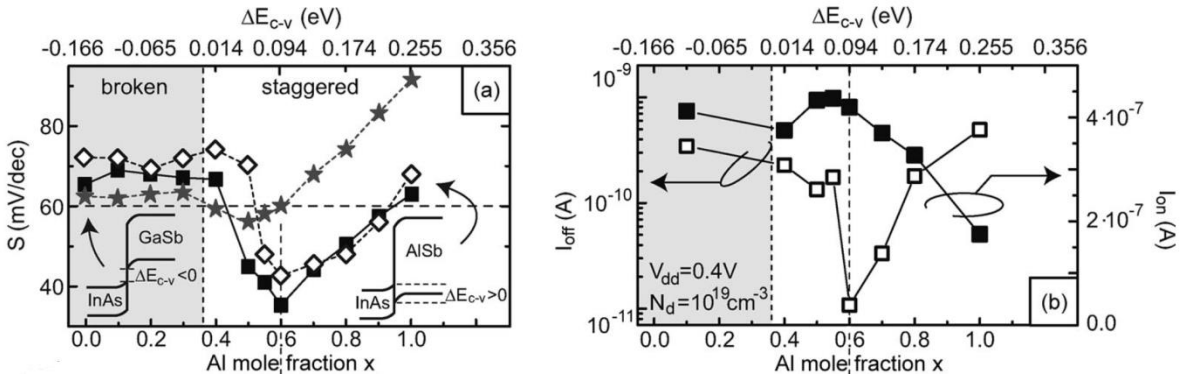

Figure 2.15 – (a) Subthreshold slope as a function of composition x of devices for different doping of NWTFET with L=20 nm, d_{ox}=1 nm, and d_{nw}=10 nm, l_{under}= 5 nm [54].

Furthermore, the formation of a heterojunction on the drain side might be an option to reduce the ambipolar tunneling current. Nevertheless, the alloy scattering effect on the degradation of carrier's mobility must be taken into account [55]. The lattice mismatching in heterojunction represents also a practical issue and results in highly defective material. For instance, a lattice mismatch of about 11% was reported from the epitaxial nanowire growth of InAs on Si [56]. Further investigations and carful choice of materials compositions are needed to achieve the best performances.

2.6. Conclusion

In this chapter, a brief physical description of tunneling mechanism in semiconductors was broached along with the broadly used semi-classical models. The non-local approach yields more precise evaluation of the tunneling current but requires the use of numerical tools. The local models are more insightful and permit the consideration of the material physical structure, nevertheless, the basis of this model's type results in a non-negligible current

overestimation. The physical description of the tunneling mechanism allowed us to develop a comprehensive study on the use and the control of tunnel transport in transistors. A detailed description of the device working principle was then carried out.

Basing on the tunneling path, the TFET can be classified in different types, each one offers a certain advantage. Besides, the TFET can take different architectures. The enhanced electrostatic control of gate all around structure is also beneficial to TFETs but only in non-confined systems. Moreover, TFET exhibits MOSFET like characteristics and can achieve low leakage current, steep subthreshold slope, efficient transconductance and high intrinsic gain. However, the ambipolarity, trap assisted tunneling and high Miller capacitance can seriously alter the device performances and impede its use for digital and analog low power applications.

Because of the different transport's physic, the TFET exhibits better immunity against SCEs than conventional MOSFETs. Nevertheless, this feature is drastically degraded beyond 30 nm, where drain induced barrier thinning (DIBT) exponentially increases. Furthermore, experimental characterization of various TFET configurations and materials show that the sub 60 mV/dec is rarely achieved, especially for silicon, while narrow bandgap materials yields higher off-current. In addition, the drain current and transconductance are still falling short of expectations.

Therefore, new practical design solutions such as high-κ dielectric materials, drain underlap, source/drain doping, gate material engineering, channel strain, heterojunctions and III-V materials have been proposed to overcome these physical limitations. A possible mixing and compromise between the enumerated solutions may lead the TFET in surpassing the advanced MOSFET performances and be a real alternative for future technology.

References

[1] E. O. Kane, “Zener tunneling in semiconductors,” Journal of Physics and Chemistry of Solids, vol. 12, pp. 181-188, Jan. 1960.

[2] K. Ahmed, M. M. Monzure Elahi, Md. Shofiqul Islam, “A Compact Analytical Model of Band-to-Band Tunneling in a Nanoscale p-i-n Diode,” International Conference on Informatics, Electronics & Vision (ICIEV), Dhaka, Bangladesh, 18-19 May 2012.

[3] B. Bhushan, K. Nayak, V. R. Rao, “DC Compact Model for SOI Tunnel Field-Effect Transistors,” IEEE Transactions on Electron Devices, vol. 59, pp. 2635-2642, Oct. 2012.

[4] Y. Taur, J. Wu, J. Min, “An Analytic Model for Heterojunction Tunnel FETs with Exponential Barrier,” IEEE Transactions on Electron Devices, vol. 62, pp. 1399-1404, May. 2015.

[5] J. K. Mamidala, R. Vishnoi, P. Pandey, “Tunnel Field-effect Transistors (TFET): Modeling and Simulation,” Wiley publishers, 2017.

[6] E. O. Kane, “Theory of Tunneling,” Journal of Applied Physics, vol. 32, pp. 83-91, Feb. 1961.

[7] J. Appenzeller, Y.M. Lin, J. Knoch, Ph. Avouris, “Band-to-band tunneling in carbon nanotube field-effect transistors,” Physical Review Letters, Vol.93, pp. 196805.1-4. Nov. 2004.

[8] ITRS Summer Meeting, Palo Alto, CA, July 11-12, 2015.

[9] G. V. Luong, et al., “Complementary Strained Si GAA Nanowire TFET Inverter With Suppressed Ambipolarity,” IEEE Electron Device Letters, vol. 37, pp. 950-953, Aug. 2016.

[10] C. Schulte-Braucks, et al., “Experimental demonstration of improved analog device performance of nanowire-TFETs,” Solid-State Electronics, vol. 113, pp. 179-183, Nov. 2015.

[11] S. Datta, H. Liu, V. Narayanan, “Tunnel FET technology: A reliability perspective,” Microelectronics Reliability, vol. 54, pp. 861-874, May. 2014.

[12] A. C. Seabaugh, Q. Zhang, “Low-Voltage Tunnel Transistors for Beyond CMOS Logic,” Proceedings of the IEEE, vol. 98, pp. 2095-2110, Dec. 2010.

[13] R. H. Fowler and L. Nordheim, “Electron Emission in Intense Electric Fields,” Proceedings of the Royal Society of London. vol. 119, pp. 173-181, May. 1928.

[14] R. W. Gurney and E. U. Condon, “Quantum Mechanics and Radioactive Disintegration,” Physical Review Journarls, vol. 33, pp. 127-140, Feb. 1929.

[15] S. D. Liang, “Quantum Tunneling and Field Electron Emission Theories,” World Scientific Publishing, Singapore, 2013.

[16] C. Zener, “A theory of the electrical breakdown of solid dielectrics,” Proceedings of the Royal Society of London, vol. 145, pp. 523-529, Jul. 1934.

[17] K. B. McAfee, E. J. Ryder, W. Shockley, and M. Sparks, “Observations of Zener Current in Germanium p−n Junctions,” Physical Review Journals, vol. 83, pp. 650-651, Aug. 1951.

[18] L. Esaki, “New Phenomenon in Narrow Germanium p-n Junctions,” Physical Review Journals, vol. 109, pp. 603-604, Jan. 1958.

[19] G. A. M. Hurkx, F. G. O’Hara, and M. P. G. Knuvers, “Modeling forward-biased tunnelling,” European Solid State Device Research Conference, pp. 793-396, Berlin, Germany, 1989.

[20] L. Esaki, “Tunneling, chapter book in: Tunneling Phenomena in Solids,” Plenum Press, New York USA, 1969.

[21] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, “A New Recombination Model for Device Simulation Including Tunneling,” IEEE Transactions on Electron Devices, vol. 39, pp. 331-338, Feb. 1992.

[22] A. Schenk, “Rigorous theory and simplified model of the band-to-band tunneling in silicon,” Solid-State Electronics, vol. 36, pp. 19-34, Jan. 1993.

[23] A. Pan and C. O. Chui, “Modeling direct interband tunneling. I. Bulk semiconductors,” Journal of Applied Physics, vol. 116, pp. 054509(1-8), Jul. 2014.

[24] J. Knoch and J. Appenzeller, “Tunneling phenomena in carbon nanotube field-effect transistors,” Physica Status Solidi (a), vol. 205, pp. 679-694, Apr. 2008.

[25] A. Pan, S. Chen, C. O. Chui, “Electrostatic Modeling and Insights Regarding Multigate Lateral Tunneling Transistors,” IEEE Transactions on Electron Devices, vol. 60, pp. 2712-2720, Sep. 2013.

[26] C. ALPER, “Modeling and optimization of Tunnel-FET architectures exploiting carrier gas dimensionality,” PhD dissertation, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, 2017.

[27] J. Min, J. Wu, Y. Taur, “Analysis of Source Doping Effect in Tunnel FETs With Staggered Bandgap,” IEEE Electron Device Letters, vol. 36, pp. 1094-1096, Oct. 2015.

[28] L. L. Chang and L. Esaki, “Tunnel triode—a tunneling base transistor,” Applied Physics Letters. Vol. 31, pp. 687-689, Sep. 1977.

[29] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai, “A band to band tunneling MOS device (B^2T-MOSFET) - A kind of “si quantum device”,” Proceeding . International Electron Devices Meeting IEDM '88. Technical Digest, pp. 402-405, 11-14 Dec 1988.

[30] T. Baba, “Proposal for surface tunnel transistors,” Japanese Journal of Applied Physics, Vol. 31, Part 2, pp. 455-457, Apr. 1992.

[31] A. Gehring, S. Selberherr, “Tunneling Models for Semiconductor Device Simulation, chapter 9 of the Handbook of Theoretical and Computational Nanotechnology,” vol. 10, American Scientific Publishers, 2006.

[32] K. Boucart, A. M. Ionescu, “Double-Gate Tunnel FET With High-κ Gate Dielectric,” IEEE Transactions on Electron Devices, Vol. 54, pp. 1725-1733, Jul. 2007.

[33] K. Boucart, A. M. Ionescu, “A new definition of threshold voltage in Tunnel FETs,” Solid-State Electronics, vol. 52, pp. 1318-1323, Sep. 2008.

[34] http://www.itrs2.net/itrs-reports.html.

[35] L. Zhang, X. Lin, J. He, M. Chan, “An Analytical Charge Model for Double-Gate Tunnel FETs,” IEEE Transactions on Electron Devices, vol. 59, pp. 3217-3223, Dec. 2012.

[36] W. Lee, W.Y. Choi, “Influence of Inversion Layer on Tunneling Field-Effect Transistors,” IEEE Electron Device Letters, vol. 32, pp. 1191- 1193, Sep. 2011.

[37] S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, “On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors,” IEEE Electron Device Letters, vol. 30, pp. 1102-1104, Oct. 2009.

[38] L. Zhang and M. Chan, “SPICE Modeling of Double-Gate Tunnel-FETs Including Channel Transports,” IEEE Transactions on Electron Devices, vol. 61, pp. 300-307, Feb. 2014.

[39] P. A. Patel, “Steep Turn On/Off "Green" Tunnel Transistors,”2010.

[40] L. Lattanzio, L. De Michielis, and A. M. Ionescu, “Electron-hole bilayer tunnel FET for steep subthreshold swing and improved ON current,” in 2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC), IEEE, pp. 259-262, Sep. 2011.

[41] C. Hu, *et al*, “Prospect of Tunneling Green Transistor for 0.1V CMOS,” IEEE International Electron Devices Meeting (IEDM), pp. 387-390, San Francisco, CA, USA, 6-8 Dec. 2010.

[42] Y. Lu, *et al*.,"Geometry dependent tunnel FET performance-dilemma of electrostatics vs. quantum confinement.", In IEEE Device Research Conference (DRC), pp. 17-18, South Bend, IN, USA, 21-23 June 2010.

[43] L. Liu, D. Mohata, S. Datta,” Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors,” IEEE Transactions on Electron Devices, vol. 59, pp. 902-908, Apr. 2012.

[44] A. Mallik, A. Chattopadhyay, “The Impact of Fringing Field on the Device Performance of a p-Channel Tunnel Field-Effect Transistor With a High-κ Gate Dielectric,” IEEE Transactions on Electron Devices, vol. 59, pp. 277-282, Feb. 2012.

[45] K. K. Bhuwalka, J. Schulze, I. Eisele, “Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering,” IEEE Transactions on Electron Devices, vol. 52, pp. 909-917, May. 2005.

[46] D. S. Yadav, D. Sharma, B. R. Raad, V. Bajaj , “Impactful Study of Dual Work Function, Underlap and Hetero Gate Dielectric on TFET with Different Drain Doping Profile for High

Frequency Performance Estimation and Optimization," Superlattices and Microstructures, vol. 96, pp. 36-46, Aug. 2016.

[47] J. S. Lee, et al., "Simulation study on effect of drain underlap in gate-all-around tunneling field-effect transistors," Current Applied Physics, vol. 13, pp. 1143-1149, Aug. 2013.

[48] M. L. Lee, *et al*., "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field effect transistors," Journal of Applied Physics, vol. 97, pp. 011101, 2005.

[49] M. Najmzadeh, K. Boucart, W. Riess, A. M. Ionescu, "Asymmetrically strained all-silicon multi-gate n-Tunnel FETs," Solid-State Electronics, vol. 54, pp. 935–941, Sep. 2010.

[50] F. Mayer, et al, "Impact of SOI, $Si_{1-x}Ge_xOI$ and GeOI substrates on CMOS compatible Tunnel FET performance," IEEE International Electron Devices Meeting IEDM 2008, San Francisco, CA, USA, 15-17 Dec. 2008.

[51] T. C. McGill, D. A. Collins, "Prospects for the future of narrow bandgap materials," Semiconductor Science and Technology, vol. 8, pp. S1-S5, 1993.

[52] S. Mookerjea, *et al.*, "Experimental demonstration of 100nm channel length $In_{0.53}Ga_{0.47}As$-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications," in 2009 IEEE International Electron Devices Meeting (IEDM), pp. 1–3, IEEE, dec 2009.

[53] G. Dewey, *et al*, "Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing," IEEE International Electron Devices Meeting (IEDM), pp. 785-788, Washington, DC, USA, 5-7 Dec. 2011.

[54] J. Knoch, J. Appenzeller, "Modeling of High-Performance p-Type III–V Heterojunction Tunnel FETs," IEEE Electron Device Letters, vol. 31, pp. 305- 307, Apr. 2010

[55] V. Venkataraman, C. W. Liu, and J. C. Sturm, "Alloy scattering limited transport of two-dimensional carriers in strained $Si_{1-x}Ge_x$ quantum wells," Applied Physics Letters, vol. 63, pp. 2795- 2797, Nov. 1993.

[56] L. C. Chuang, M. Moewe, C. Chase, N. P. Kobayashi, C. Chang-Hasnain, “Critical diameter for III-V nanowires grown on lattice-mismatched substrates,” Applied Physics Letters, vol. 90, pp. 043115, Jan. 2007.

CHAPTER 3:

Semi-analytical modeling of the VSG TFET

3.1. Introduction

The recent demonstrations of the tunnel field effect transistor performances and viability on digital and analog circuits make of this non-conventional device as a potential alternative to classical MOSFET of which the physical limitations impede the fulfillment of the technology roadmap [1-9]. Compact and continuous models that could be applied to both subthreshold and superthreshold working domain are growingly needed. Such models are useful for understanding device working and for circuit simulation. Also, all these models are directly dependent on the potential profile as a base to calculate the current. In point TFETs, tunneling effect occurs in channel junctions, source/channel and drain/channel if ambipolarity is considered. In this case, the development of an accurate potential profile model is complex due to the additional processes that have to be taken into account, such as depletion, fringing effect on source drain extensions (SDE) and the impact of high lateral field near junctions [10-15]. The complex tunneling barrier shape in TFET device supposes that non-local approach based on the WKB approximation and the Landauer formula is more appropriate [16-18]. Nevertheless, the exact profile of the barrier cannot be used in the elaboration of analytical models and for this reason, an arbitrary shape is adopted yielding the same issues of the local models or implying the use of numerical integration methods [9, 16]. Indeed, the assumption of constant electric field used in local tunneling models overestimates the current and produces a non-zero current at equilibrium. However, this can be resolved by the introduction of the Fermi occupancy factor difference between the source and the drain [15].

Recently, several analytical models have been developed to investigate TFET device [13-20]. However, in the majority of these models, the simplified Kane's generation rate is used in which the total electric field is replaced by an average one based on the tunneling distance or tunneling window. Nevertheless, this approach does not evaluate the generation rate over the entire tunneling barrier and thus, fails to reproduce the characteristic response profile. Besides, these models yield complex expressions making their mathematical derivation an intractable task. The derivative formulas are primordial for the extraction of many parameters and Figures of Merit (FOMs) used for the assessment of the device performances. Furthermore, a big part of the elaborated models do not take into account the drain modulation. In this context, new analytical and continuous models that capture

the physics of tunneling transport accurately and efficiently are required and suitable to be implemented in commercial simulators to study and design TFET-based nanoelectronic circuits.

In this chapter, undoped vertical surrounding gate TFET device with high-κ dielectric stack is considered. A continuous semi-analytical model is developed from mathematical integration over channel length of complete Kane generation rate expression for direct local tunneling. This integral has the merit of preserving the spatial distribution of the generation rate, which yields accurate response. Both ambipolarity and dual modulation effects are investigated. Electric field expression is derived from accurate solution of Poisson's equation using Bessel-Fourier series. The analog/RF parameters and various FOMs of the device are deduced from the proposed drain current model. Moreover, the role of gate dielectric material engineering in improving the analog/RF performance is investigated. The obtained analytical results have been validated using numerical simulations, where a good agreement is recorded for wide range of design parameters [21].

3.2. Current model derivation

The considered device in this work is a vertical surrounding gate structure as exposed in fig 3.1. The source/drain extensions are symmetric and heavily doped with a value around 10^{20} cm^{-3}. The introduction of the high dopant concentration is motivated by the attenuation of the depletion effect [22] and attaining high built-in potential, which in turn leads to significant tunneling generation. With a channel length of 100 nm, the short channel effects are considerably reduced and the assumption of an intrinsic body is well justified, where only mobile charges define the electrostatic distribution [23]. However, both charge types have to be taken into account in order to obtain a large transfer characteristic over positive and negative gate supply. The dielectric gate stack is composed of a 2 nm thickness silicon oxide and a 1 nm high-κ dielectric material to reduce gate current leakage. The 2-D numerical simulations performed to validate the current model are based on Boltzmann statistics and drift-diffusion transport. In addition, we adopted Kane direct tunneling model to support the tunneling generation phenomenon.

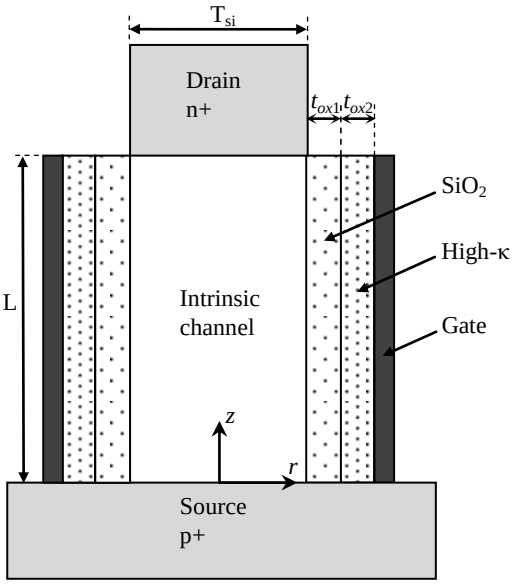

Figure 3.1 – Cross sectional view of the vertical surrounding gate TFET structure (L=100 nm, N_{AS}=N_{DD}=10^{20} cm^{-3}, t_{ox1}=2 nm, t_{ox2}=1 nm).

The first step in the model derivation is to extract the potential profile over the channel by solving the 2-D Poisson's equation, which can be expressed in cylindrical coordinates as:

$$\frac{\partial^2\psi}{\partial r^2}+\frac{1}{r}\cdot\frac{\partial\psi}{\partial r}+\frac{\partial^2\psi}{\partial z^2}=-\frac{q}{\varepsilon_{Si}}\rho \tag{3.1.a}$$

$$\rho=\begin{cases}-n_i e^{\left(\frac{\psi-V_{qn}}{V_t}\right)} & \text{for} \quad V_{gs}\geq 0\\ n_i e^{\left(\frac{-\psi+V_{qp}}{V_t}\right)} & \text{for} \quad V_{gs}<0\end{cases} \tag{3.1.b}$$

where ψ represents the 2-D electrostatic potential, ε_{Si} the silicon dielectric constant, q the electron charge, n_i the intrinsic carrier concentration, V_t the thermal voltage and ρ the channel mobile charge concentration.

Depending on gate supply polarity, only majority carriers in the channel assuring the current transport are taken into account. Indeed the neglecting of the minority carriers has no consequence even near charge equilibrium, where the center channel potential varies linearly. The quasi-Fermi level V_q included in boundary conditions is assumed to be constant over the radius, and varies from 0 at the source side to V_{ds} at the drain side [24]. In the

channel middle, the quasi-Fermi levels associated to both carriers' types V_{qn} and V_{qp} equal respectively V_{ds} and 0. To solve Poisson's equation, it needs to be projected onto two components [24], i.e. a 1D Poisson equation where the potential $V_c(r)$ represents the solution of Gauss's law in a disk of finite charge density, while the potential $U(z,r)$ in the 2-D Laplace equation represents the solution of Gauss's law in a finite cylinder of null charge density. The sum of these two terms equals the total potential distribution in the channel and are expressed with boundary conditions as:

$$\frac{\partial^2 V_c}{\partial r^2}+\frac{1}{r}\cdot\frac{\partial V_c}{\partial r}=-\frac{q}{\varepsilon_{Si}}\rho \tag{3.2.a}$$

$$\begin{cases}\left.\dfrac{\partial V_c(r)}{\partial r}\right|_{r=a}=\dfrac{C_{ox}}{\varepsilon_{Si}}\left[V_g^*-V_c(a)\right]\\ \left.\dfrac{\partial V_c(r)}{\partial r}\right|_{r=0}=0\end{cases} \quad \text{with} \quad V_g^*=V_{gs}-V_{fb} \tag{3.2.b}$$

$$\frac{\partial^2 U}{\partial r^2}+\frac{1}{r}\cdot\frac{\partial U}{\partial r}+\frac{\partial^2 U}{\partial z^2}=0 \tag{3.3.a}$$

$$\begin{cases}\left.\dfrac{\partial U(z,r)}{\partial r}\right|_{r=a}=\dfrac{C_{ox}}{\varepsilon_{Si}}\left[-U(z,a)\right]\\ \left.\dfrac{\partial U(z,r)}{\partial r}\right|_{r=0}=0\end{cases} \tag{3.3.b}$$

$$\begin{cases}U(0,r)=V_{biS}-V_c=-Vt\ln\left(\dfrac{N_{AS}}{n_i}\right)-V_c\\ U(L,r)=V_{biD}+V_{ds}-V_c=Vt\ln\left(\dfrac{N_{DD}}{n_i}\right)+V_{ds}-V_c\end{cases} \tag{3.3.c}$$

$$C_{ox}=\frac{\varepsilon_{ox}}{a\ln(1+t_{oxeff}/a)} \text{ with } t_{oxeff}=t_{ox1}+t_{ox2}\,\varepsilon_{ox1}/\varepsilon_{ox2} \quad \text{and} \quad a=t_{si}/2 \tag{3.3.d}$$

where V_{fb} represents the flat band voltage, C_{ox} the oxide capacitance, ε_{ox} the silicon oxide dielectric constant and t_{oxeff} the effective oxide stack thickness (EOT) depending on the two layers thicknesses (the oxide layer and the high-κ layer) and their dielectric constants. It is

noted that near the channel center, the 2-D potential component is neglected so only the 1D component is involved in the charge concentration expression. By following Chambré method [25] for resolving Poisson-Boltzmann equation and using boundary conditions (3.2.b), the channel center potential upon the gate polarity is given by:

$$V_c = V_{ds} + V_t \log\left(\frac{8\beta}{\delta(\beta - r^2)^2}\right) \quad \text{for} \quad V_{gs} \geq 0 \tag{3.4.a}$$

$$V_c = V_t \log\left(\frac{\delta(\beta - r^2)^2}{8\beta}\right) \quad \text{for} \quad V_{gs} < 0 \tag{3.4.b}$$

where $\delta = qn_i / \varepsilon_{Si} V_t$, the constant β is obtained by substituting (3.4) in (3.2.b), which results in the following formulas:

$$\frac{C_{ox}}{\varepsilon_{si}}\left(V_g^* - V_{ds} - V_t \ln\left(\frac{8\beta}{\delta\left(\beta - a^2\right)^2}\right)\right) = \frac{4aV_t}{\left(\beta - a^2\right)} \quad \text{for} \quad V_{gs} \geq 0 \tag{3.5.a}$$

$$\frac{C_{ox}}{\varepsilon_{si}}\left(V_g^* - V_t \ln\left(\frac{\delta\left(\beta - a^2\right)^2}{8\beta}\right)\right) = \frac{4aV_t}{\left(a^2 - \beta\right)} \quad \text{for} \quad V_{gs} < 0 \tag{3.5.b}$$

Using the boundary conditions in (3.3.b) and (3.3.c), the solution of the 2-D Laplace equation based on Bessel-Fourier series can be expressed as [26]:

$$U(z,r) = \sum_{n=1}^{\infty} \frac{J_0(\lambda_n r)}{\sinh(\lambda_n L)}\left[A_n \sinh(\lambda_n (L - z)) + B_n \sinh(\lambda_n z)\right] \tag{3.6}$$

with λ_n being the n[th] root of the Robin condition $\lambda_n / C = J_0(\lambda_n a) / J_1(\lambda_n a)$ and $C = C_{ox} / \varepsilon_{si}$ [27]. The Bessel coefficients A_n and B_n are given by [26]:

$$A_n = \frac{2J_1(\lambda_n a)}{\lambda_n a\, J_0^2(\lambda_n a)(1 + C^2 / \lambda_n^2)}\left(V_{biS} - V_C\right) \tag{3.7.a}$$

$$B_n = \frac{2J_1(\lambda_n a)}{\lambda_n a\, J_0^2(\lambda_n a)(1 + C^2 / \lambda_n^2)}\left(V_{biD} + V_{ds} - V_C\right) \tag{3.7.b}$$

By deriving the potential expression over the length and the radius dimensions, the total electric field expression is deduced. However, the channel potential (3.4) is neglected in the

transversal field component in order to simplify the following analytical integration. The total electric field expression is divided into two components corresponding to both source and drain sides as indicated in (3.8), and hence to calculate separately the tunneling current in each junction so that the ambipolarity behavior can be obtained.

$$\begin{cases} E_S = \left[\sum_{n=1}^{\infty} \frac{\lambda_n^2 A_n^2 \left(J_0^2(\lambda_n r) + J_1^2(\lambda_n r) \right)}{4\sinh(\lambda_n L)} \exp\left(2\lambda_n (L-z)\right) \right]^{1/2} \\ E_D = \left[\sum_{n=1}^{\infty} \frac{\lambda_n^2 B_n^2 \left(J_0^2(\lambda_n r) + J_1^2(\lambda_n r) \right)}{4\sinh(\lambda_n L)} \exp\left(2\lambda_n z\right) \right]^{1/2} \end{cases} \tag{3.8}$$

At this stage, even if the channel potential at the center is accurately modeled, a good part of the electrostatic potential at junctions may be lost due to the numerous applied assumptions and simplifications.

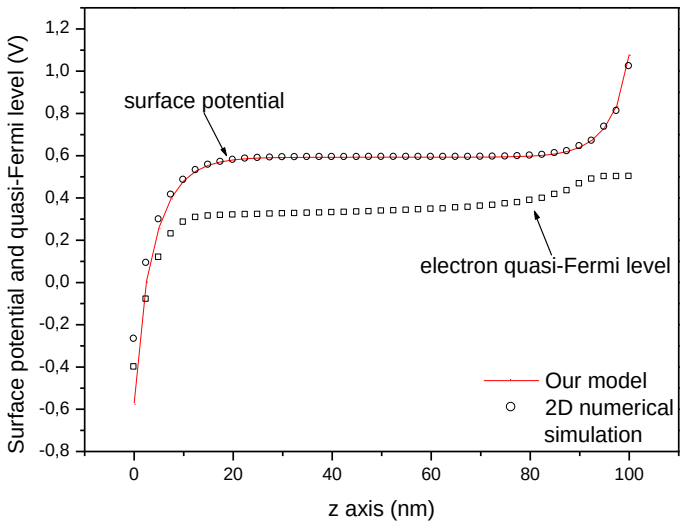

Figure 3.2 – Surface potential and quasi-Fermi level for T_{si}=10 nm, EOT=3 nm, V_{gs}=0.5 V and V_{ds}=0.5 V.

The first assumption used to explicitly solve Poisson's equation neglects the 2-D potential part in the charge concentration term, which is valid only near the channel center [24-28]. Secondly, simulations show that the quasi-Fermi levels included in boundary conditions

(3.3.c) differ from their ideal values as shown in fig 3.2. In addition, the channel potential V_c is assumed to be constant over the radius in the integrals expressions used to obtain the Bessel coefficients (3.7).

As mentioned above, the depletion and fringing effect on the source/drain extensions have a consequent impact on junctions' potential. These effects are directly dependent on the voltage supply of both drain and gate terminals. It should be mentioned that many works have included during their modeling procedures the depletion and fringing field effect on different structure types [10, 11, 19, 29]. Nevertheless, the remarkable lack of accuracy as depicted by the outcomes of the aforementioned works makes the addition of fitting parameters inevitable to adjust the boundary potential. Although in our case, the depletion effect is neglected due to high SDEs doping, numerical simulations show an important linear variation in boundary potentials at the silicon interface, which attenuates in depth direction. As the use of additional parameters seems necessary, it is preferable to avoid such effects modeling and directly include fitting parameters and functions at the level of the final obtained expressions to simplify their extraction. Consequently, a correction potential V_p is added to the boundary potentials (3.3.c). Guided by the numerical fitting, we observe that such potential depends only on geometrical parameters.

Since the analytical integration of the tunneling generation rate over the radius can be difficult under some situations, only the surface total electric field in (3.8) is taken into consideration. Moreover, the integration process of a large number or infinite series order is an intractable task, which justifies the simplification of the expressions (3.8) by focusing on the first series' order given by:

$$E_S = A\exp\left(-\lambda z\right) \tag{3.9.a}$$

with $$A = \frac{-\lambda\left(1+J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}}\exp(\lambda L)}{2\sinh(\lambda L)}\left(V_p + V_{biS} - V_c\exp\left(V_{cn}\left(1-\frac{V_c}{V_g^*}\right)\right)\right)$$

$$E_D = B\exp\left(\lambda z\right) \tag{3.9.b}$$

with $B = \frac{\lambda\left(1+J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}}}{2\sinh(\lambda L)}\,\mathrm{abs}\left(-V_p + V_{biD} + V_{ds} - V_c \exp\left(V_{cp}\left(1-\frac{V_c}{V_g^*}\right)\right)\right)$

The exponential term describes the dual modulation effect. During gate modulation regime, we have $V_c = V_g^*$ so the exponential term equals one, otherwise the channel to gate potential ratio determines the amount of drain modulation on tunneling generation corrected by the coefficients V_{cn} and V_{cp}, whose values vary around one and are dependent on the geometrical parameters and the drain supply for V_{cn}.

These simplified electric field expressions are analogous to the exponential surface potential distribution used in pseudo-2-D potential models [10, 13, 18], as well as the root of the Robin condition, which is inversely equivalent to the characteristic length. This parameter defines the barrier bending profile or more specifically the electric field amplitude. Near junctions, the effect of high lateral field can't be neglected; which means that the classical MOSFET interface boundary condition (3.3.b) used to extract the Robin condition roots is no more valid. In [20], the first order electric field expression is multiplied by a fitting coefficient to compensate the limitation of Fourier series to a one order expression. Moreover, the dependence of the characteristic length on gate bias is demonstrated and modeled in [12]. In order to fulfill a satisfactory accuracy of the potential distribution and to reduce the total electric field series expression to the first order, a dimensionally dependent fitting function is used in the Robin condition as $C_p C/\lambda = J_1(\lambda a)/J_0(\lambda a)$ with C_p defined by:

$$C_p = \frac{(\alpha_1 t_{si} + \beta_1)}{((\alpha_1 t_{si} + \beta_1)^2 + (\varepsilon_{ox2} + \pi)^2)} + \mu e^{(-\mu(\alpha_2 t_{si} + \beta_2))} + \nu e^{(\rho(\alpha_2 t_{si} + \beta_2))} \qquad (3.10)$$

where all the parameters can be numerically fitted. The Kane tunneling generation rate used in this work is given by $G_T = A_k E^{G_k} \exp\left(-B_k/E\right)$ [30], where A_k= 3.3679x10^{21}, B_k = 2.5253x10^7 for silicon material, and G_k = 2 since only direct tunneling process is considered. By replacing the total electric field E by the expressions (3.9.a) and (3.9.b), the generation rate for each channel side becomes:

$$G_{TS} = A_k (A^2 \exp(-2\lambda z)) \exp\left(\frac{-B_k \exp(\lambda z)}{A}\right) \quad (3.11.a)$$

$$G_{TD} = A_k (B^2 \exp(2\lambda z)) \exp\left(\frac{-B_k \exp(-\lambda z)}{B}\right) \quad (3.11.b)$$

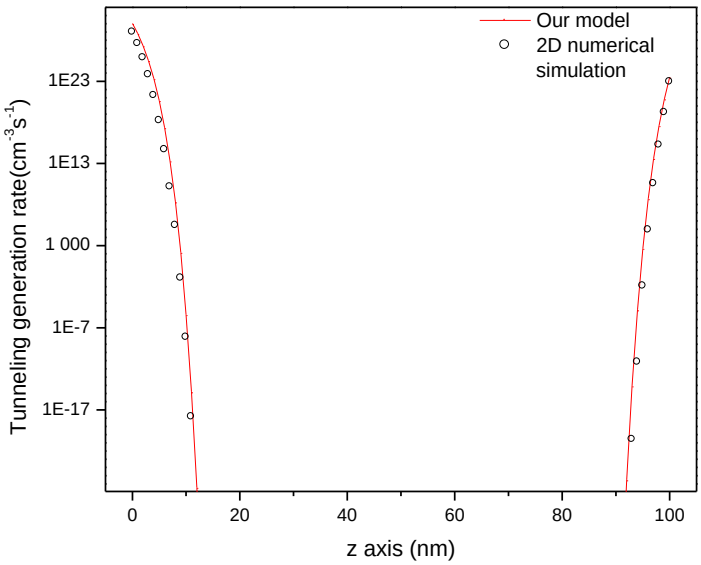

Figure 3.3 – Tunneling generation rate distribution for T_{si}=10 nm, EOT=3 nm, V_{ds}=0.5 V and V_{gs}=0.5 V.

Fig 3.3 shows the good agreement of the modeled tunneling generation rate with respect to the simulated responses. As expected, the maximum rate is located at junctions where the major tunneling process occurs and drops drastically when receding from the channel boundaries. Hence, it is possible to get the total tunneling current by summing the integrals of the generation rate equations over channel length and radius at junction locations as illustrated below:

$$I_T = I_{TS} + I_{TD} = q2\pi \int_0^L \int_0^a r\left(G_{TS} + G_{TD}\right) dr dz \quad (3.12)$$

$$I_{TS} = -q\pi a^2 A_k \left(\frac{B_k^2 \,\mathrm{Ei}\left(\frac{-B_k}{A}\right) + A\exp\left(\frac{-B_k}{A}\right)\left(B_k - A\right)}{2D\lambda} \right) \tag{3.13.a}$$

$$I_{TD} = -q\pi a^2 A_k \left(\frac{\left(B_k^2 \,\mathrm{Ei}\left(\frac{-B_k e^{-\lambda L}}{B}\right) + B\exp\left(\frac{-B_k e^{-\lambda L}}{B} + 2\lambda L\right)\left(B_k e^{-\lambda L} - B\right)\right)}{2D\lambda} \right) \tag{3.13.b}$$

$$\text{with } D = \left(\frac{\lambda}{(\eta(t_{si})t_{oxeff} + \sigma(t_{si}))} \right)^{\tau} \left(1 + \frac{\Delta_r}{\left(1 + \left(\frac{V_g - V_{gm}}{\iota}\right)^2\right)^2} \right) \tag{3.13.c}$$

with D is a fitting function that evaluates the depth of the tunneling process when only the surface electric field is involved. The second term is a correction function that permits the reduction of the relative error against numerical simulation at the vicinity of 0.1 % during the gate modulation, where V_{gm} is the gate voltage and Δ_r the relative error corresponding to the minimum current.

The next figures validate the current model for different configurations and voltage supplies. As it can be deduced from the model, reducing the oxide layer thickness will consequently raise the oxide capacitance, the electric field and the tunneling current in turn as illustrated in fig 3.4a and fig 3.5b. In an analogous manner, the reduction of channel radius leads to an increase in the tunneling current.

The ambipolarity behavior is well described, as well as the dual modulation effect. The tunneling current in the drain side increases relatively to drain bias and shifts the minimum current forward with gate voltage. Furthermore, it is clearly highlighted that during the gate modulation, the tunneling process in source side is totally independent of the drain bias. The dual modulation effect is also described in fig 3.5b, where for low drain bias; the tunneling in source side is controlled by the drain modulation. The channel potential varies linearly with the drain bias until the drain boundary potential exceeds the channel potential.

Then, the regime switches to the gate modulation, where the constant gate bias fixes the tunneling near the source side and raises its value at the drain side.

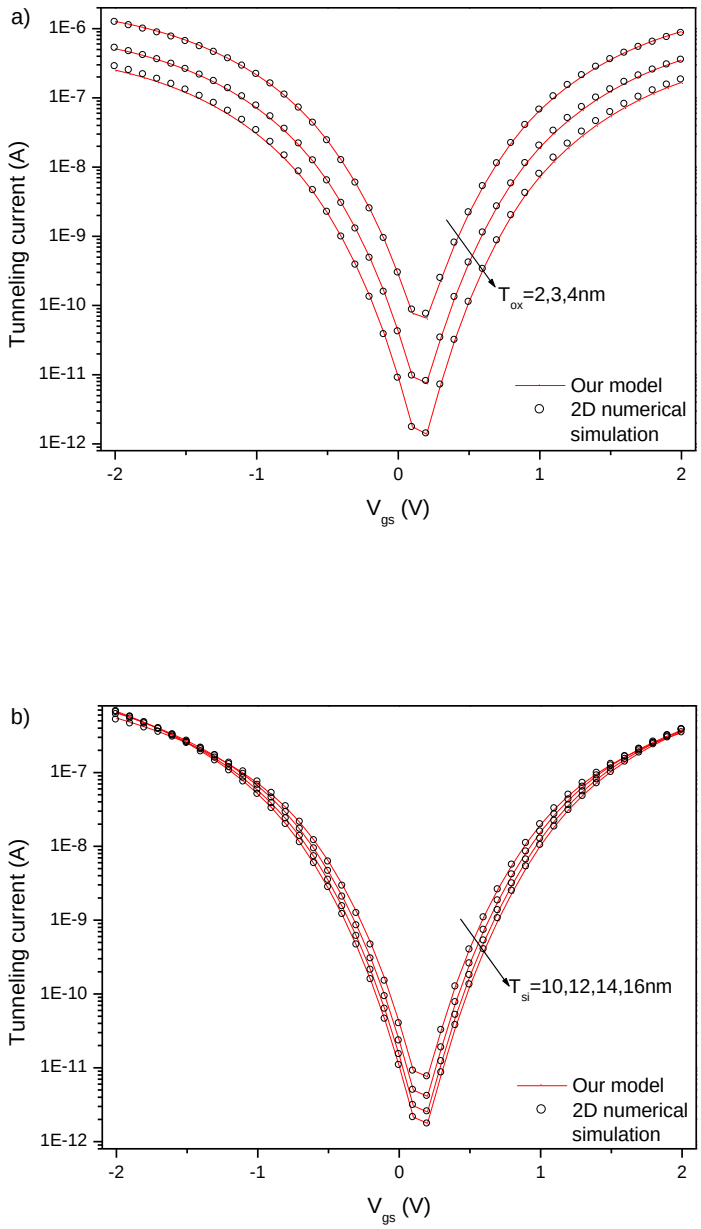

Figure 3.4 – Tunneling current versus gate bias for (a) different oxide thicknesses (T_{si}=10 nm and V_{ds}=0.5 V) and (b) different channel diameters (EOT=3 nm and V_{ds}=0.5 V).

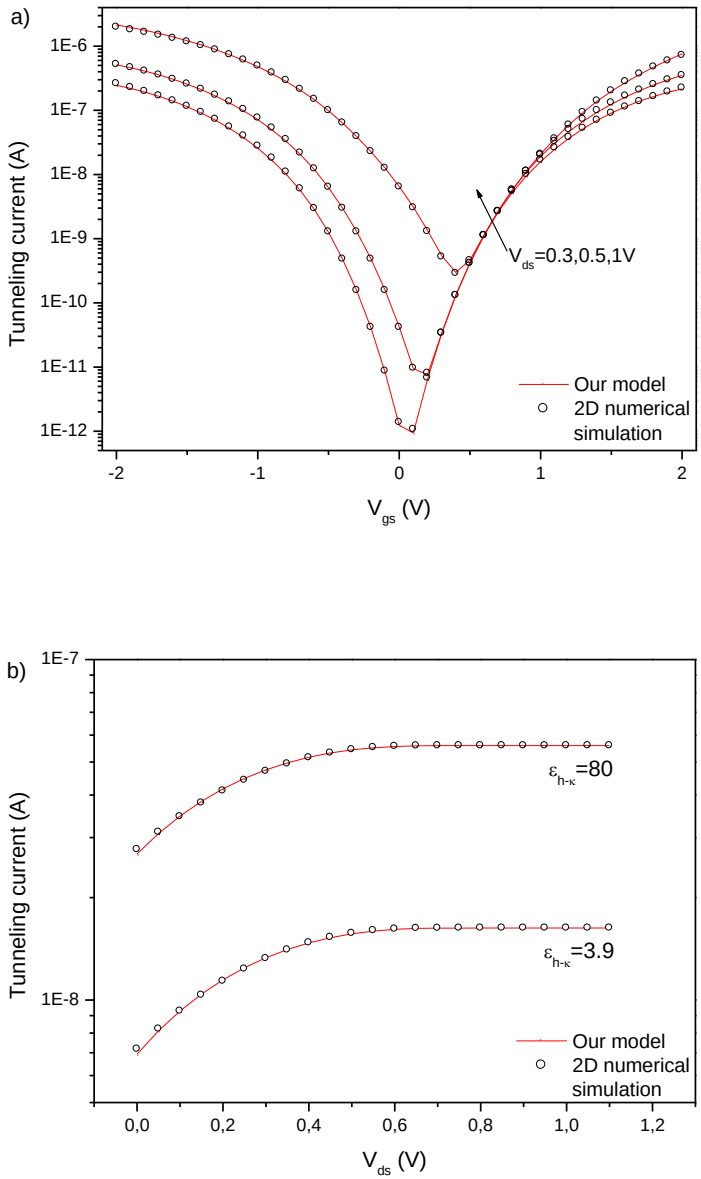

Figure 3.5 – Tunneling current versus (a) gate bias for different drain biases (T_{si}=10 nm and EOT=3 nm). (b) drain bias for different high-κ values, (T_{si}=12 nm and V_{gs}=1 V).

The next step consists in the derivation of the current expression with respect to gate and drain supplies with the aim of extracting different analog/RF parameters. It is worth mentioning that only the source tunneling current is considered.

$$\frac{\partial I_{TS}}{\partial V_{gs}} = q\pi a^2 A_k \left(\frac{A e^{\left(\frac{-B_k}{A}\right)}}{D\lambda} \frac{\partial A}{\partial V_{gs}} \right) \tag{3.14}$$

with $\frac{\partial A}{\partial V_{gs}} = -\lambda \left(1 + J_1^2(\lambda a) / J_0^2(\lambda a)\right)^{\frac{1}{2}} \left(\frac{V_{cn} V_c \left(V_g^* \frac{\partial V_c}{\partial V_{gs}} - V_c \right)}{V_g^{*2}} - \frac{\partial V_c}{\partial V_{gs}} \right) \exp\left(V_{cn} \left(1 - \frac{V_c}{V_g^*} \right) \right)$

and $\frac{\partial V_c}{\partial V_{gs}} = \left(1 + \frac{4a\beta}{C\left(\beta^2 - a^4\right)} \right)^{-1}$

The last equation is obtained by the derivation of the expression (3.4.a) and then by replacing the derivative of β by:

$$\frac{\partial \beta}{\partial V_{gs}} = \left(\frac{-\beta\left(\beta - a^2\right)}{V_t\left(\beta + a^2\right)} \right) \frac{\partial V_c}{\partial V_{gs}}$$

Following the same methodology, the derivative with respect to the drain supply is given by:

$$\frac{\partial I_{TS}}{\partial V_{ds}} = q\pi a^2 A_k \left(\frac{A e^{\left(\frac{-B_k}{A}\right)}}{D\lambda} \frac{\partial A}{\partial V_{ds}} \right) \tag{3.15}$$

where $\frac{\partial A}{\partial V_{ds}} = \lambda \left(1 + J_1^2(\lambda a) / J_0^2(\lambda a)\right)^{\frac{1}{2}} \left(V_c \frac{\partial V_{ce}}{\partial V_{ds}} + V_{ce} \frac{\partial V_c}{\partial V_{ds}} \right)$

and

$$\frac{\partial V_c}{\partial V_{ds}} = \left(1 + \frac{C\left(\beta^2 - a^4\right)}{4a\beta} \right)^{-1} \text{ and } \frac{\partial \beta}{\partial V_{ds}} = \left(\frac{\left(\beta - a^2\right)^2}{4aV_t} \right) \frac{\partial V_c}{\partial V_{ds}}$$

Here, the fitting function V_{ce} replaces the exponential term since the drain bias dependent parameter V_{cn} is difficult to model and by doing so the derivative expression is simplified. The numerical fitting provides the following formula $V_{ce} = 4\left(V_c + c_1\right)^{-1/4} + c_2 V_{ds} + c_3$.

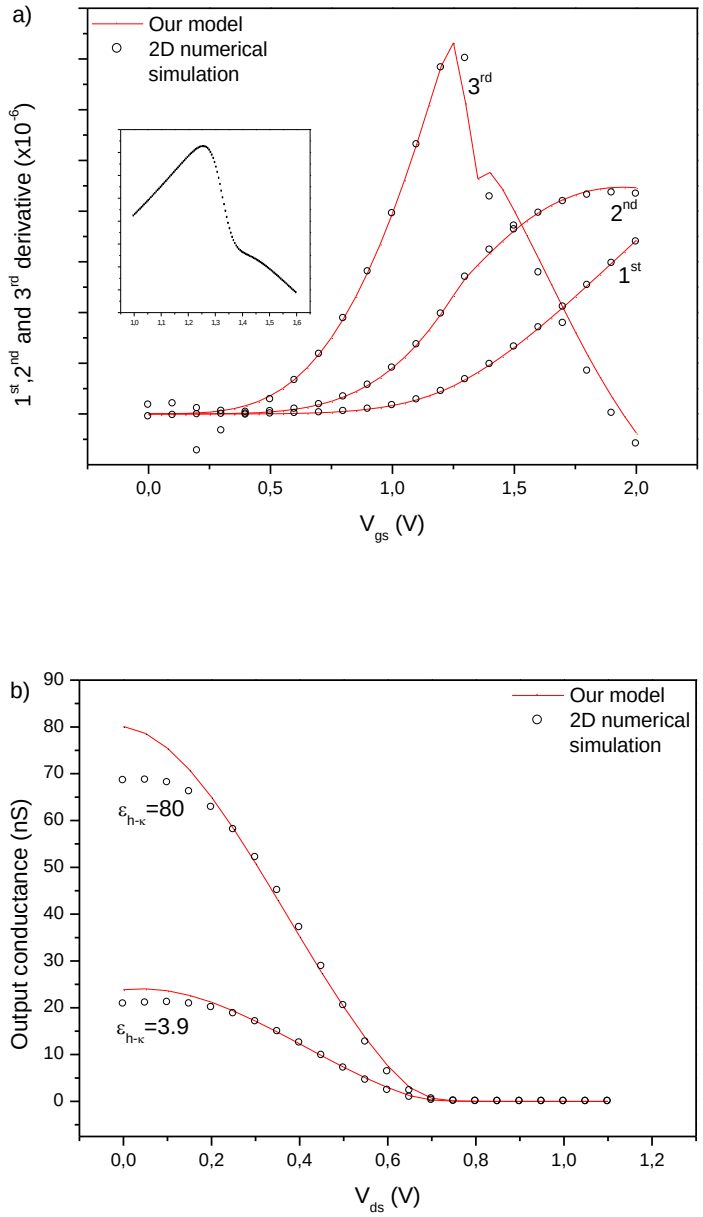

Figure 3.6 – (a) Multiple current derivative degrees with respect to the applied gate voltage, (T_{si}=14 nm, EOT=3 nm and V_{ds}=1 V), the inset figure illustrates with more accuracy the simulated third derivative (b) First current derivative with respect to the applied drain voltage (T_{si}=12 nm and V_{gs}=1 V).

The transition from the gate modulation to the drain modulation of the tunneling barrier is reflected in the third derivative (fig 3.6a). This transition occurs smoothly over an interval of

gate bias. The start point corresponds to the maximum of the third derivative while the end point is revealed by a kink effect. On the basis of the previous elaborated expressions, any derivative degree can be obtained with a good agreement in comparison to its numerical counterpart, especially during the gate modulation as depicted in fig 3.6. Nevertheless, the exponential term accounting for the drain modulation needs to be accurately modeled. One of the important parameters based on the current derivative formula and adopted to assess the TFET performance is the subthreshold slope (SS) expressed by:

$$SS = \frac{\partial V_{gs}}{\partial \log_{10}(I_T)} = \log(10)\frac{\left(I_{TS} + I_{TD}\right)}{\partial I_{TS}/\partial V_{gs} + \partial I_{TD}/\partial V_{gs}} \tag{3.16}$$

with $\frac{\partial I_{TD}}{\partial V_{gs}} = q\pi a^2 A_k \left(\frac{Be^{\left(2\lambda L - \frac{B_k \exp(-\lambda L)}{B}\right)}}{D\lambda} \frac{\partial B}{\partial V_{gs}} \right)$

where $\frac{\partial B}{\partial V_{gs}} = -\frac{\lambda\left(1 + J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}}}{2\sinh(\lambda L)}$

It is noticed that the derivative of the term B is limited to the gate modulation regime for which the exponential term equals one. The next figures illustrate the variation of the minimum subthreshold slope and the I_{on}/I_{off} current ratio for different dimensions and drain supplies (I_{on} @ V_{gs}=1 V and I_{off}=I_{Tmin}). As aforementioned, the reduction of the channel diameter and the oxide thickness enhance the on-current. Unfortunately, the off-current is increased as well with an amount that exceeds the on-current augmentation magnitude. Consequently, the I_{on}/I_{off} current ratio as well as the SS_{min} degrade for reduced channel diameter and oxide thickness (fig 3.7a, b). Furthermore, these degradations are accentuated with drain bias increase. Such major alterations are attributed to the large bandgap of silicon and the enhanced ambipolar current. In practice, many solutions are available to improve the TFET performances. For this purpose, the validity of the developed model for any material may be useful to explore the impact of material engineering. Nevertheless, as our model is based on local tunneling approach, it is not suitable to heterostructure TFETs where non-local model should be applied [17, 18].

In order to get a more reliable modeling framework, an adaptation of the model to describe the SCEs is necessary. Indeed, the model derivation is based on the assumption that $\sinh(\lambda L)\approx\exp(\lambda L)/2$, which is correct only for long channel lengths. Furthermore, the drain induced barrier thinning yields modification of the electrostatic distribution which results in

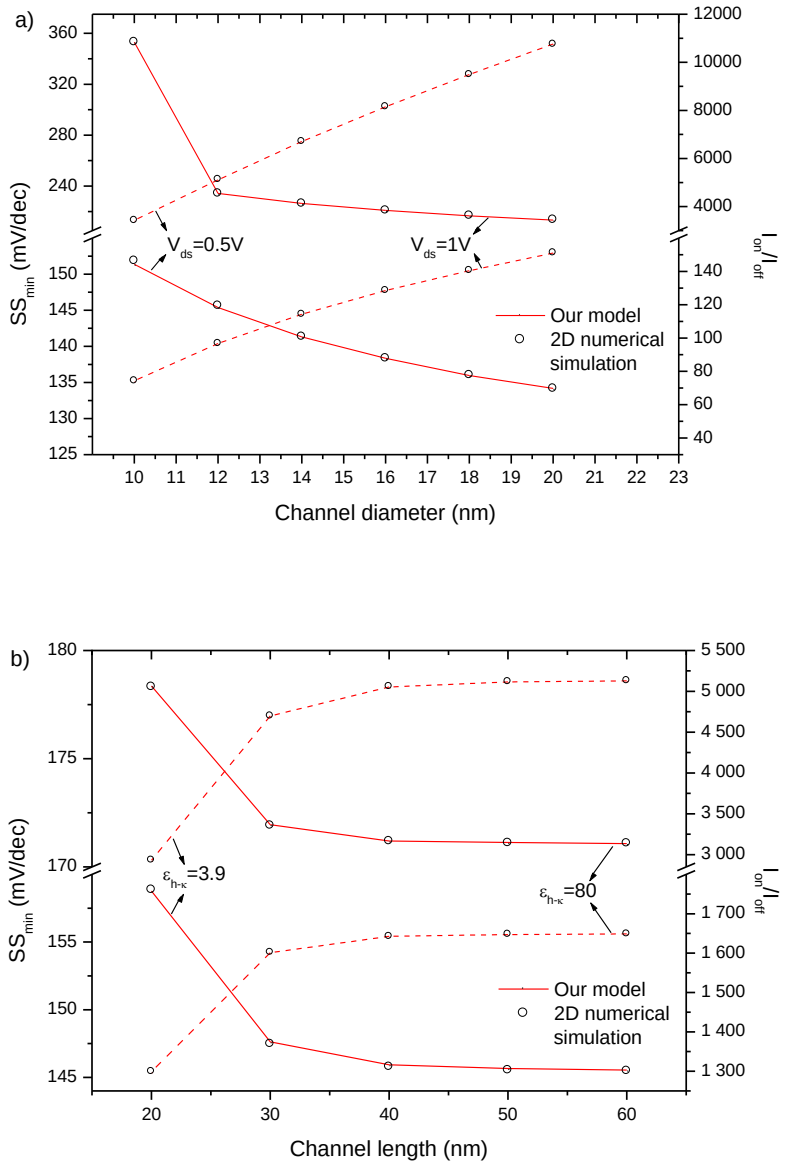

Figure 3.7 – (a) SS_{min} (solid) and I_{on}/I_{off} (dashed) as a function of channel diameter for different drain biases, (EOT=3 nm and L=100 nm) (b) SS_{min} (solid) and I_{on}/I_{off} (dashed) as function of channel length for different high-κ dielectric constant (T_{si}=12 nm and V_{ds}=0.5 V).

higher lateral electric field. This implies the introduction of the length effect on the root of the Robin condition λ [31]. In order to avoid additional modeling complexity, the impact of length variation is added to the parameters D and V_p by means of a fitting coefficient expressed by $1+\alpha^{'}\exp(\beta^{'}L)$. This solution gives a good agreement of the model with the numerical results as illustrated in Fig.7b.

As reported in literature [23, 31], the TFET exhibits a good immunity against SCEs while this feature is drastically degraded beyond 30 nm. The subthreshold slope as well as I_{on}/I_{off} are degraded in an exponential manner as depicted in fig.7b. It is noticed that the direct and trap assisted tunneling from the source to the drain that become possible for lengths approaching 20nm are not taken into account, such tunneling may further degrade the device performances [9]. However, the high-κ layer attenuates the SCEs where the SS_{min} varies around 4 % for high dielectric layer with a constant value of 80 and 9 % for a device without high dielectric layer.

3.3. Results and discussion

This section is composed of two parts. The first subsection is dedicated to the presentation of the analog/RF measures while the second part is reserved to the analysis of different linearity criteria.

3.3.1. Analog/RF parameters

The investigation of scaling capability, device performance and linearity in high frequency regime is a mandatory requirement for circuit design purposes. The TFET paradigm has been considered as a competitive alternative to MOSFET devices when adopted for analog/RF applications. The performance assessment is achieved through the compact modeling of analog/RF parameters jointly with FOMs analysis [32, 33]. The next representations depict diverse analog/RF criteria for different geometrical parameters in the gate modulation mode (V_{gs}=V_{ds}=1 V). The transconductance, defined as $\partial I_{ds} / \partial V_{gs}$, is provided in fig 3.8a as a function of the channel diameter for different high-κ values. Similarly to the case of the current, reducing the channel or the effective oxide thickness increases the transconductance. However, an attenuation of the high-κ layer effect is observed for a value

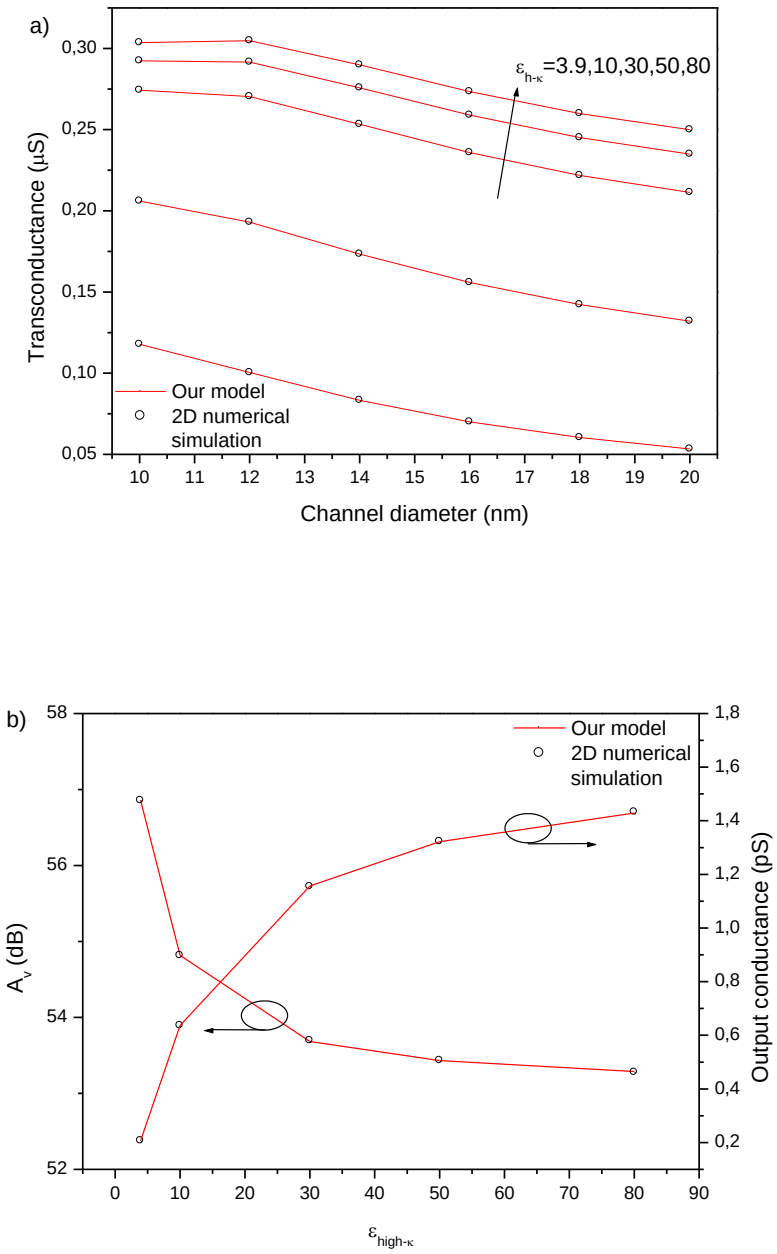

Figure 3.8 – (a) Transconductance as a function of channel diameter. (b) Intrinsic gain and output conductance as functions of the high-κ dielectric constant for T_{si}=12 nm, V_{ds}=1 V and V_{gs}=1 V.

of 10 nm. Likewise, the output conductance, defined as $\partial I_{ds} / \partial V_{ds}$, has an increasing tendency with respect to the high-κ dielectric value (fig 3.8b). It is noted that even if the

TFET transconductance is relatively low with respect to MOSEFTs, the output conductance is as much lower, leading consequently to an acceptable intrinsic gain expressed as $A_v = G_m / G_d$. However, the impact of the high-κ layer is more pronounced on G_d than G_m, which results in the degradation of the gain as highlighted in fig 3.8b.

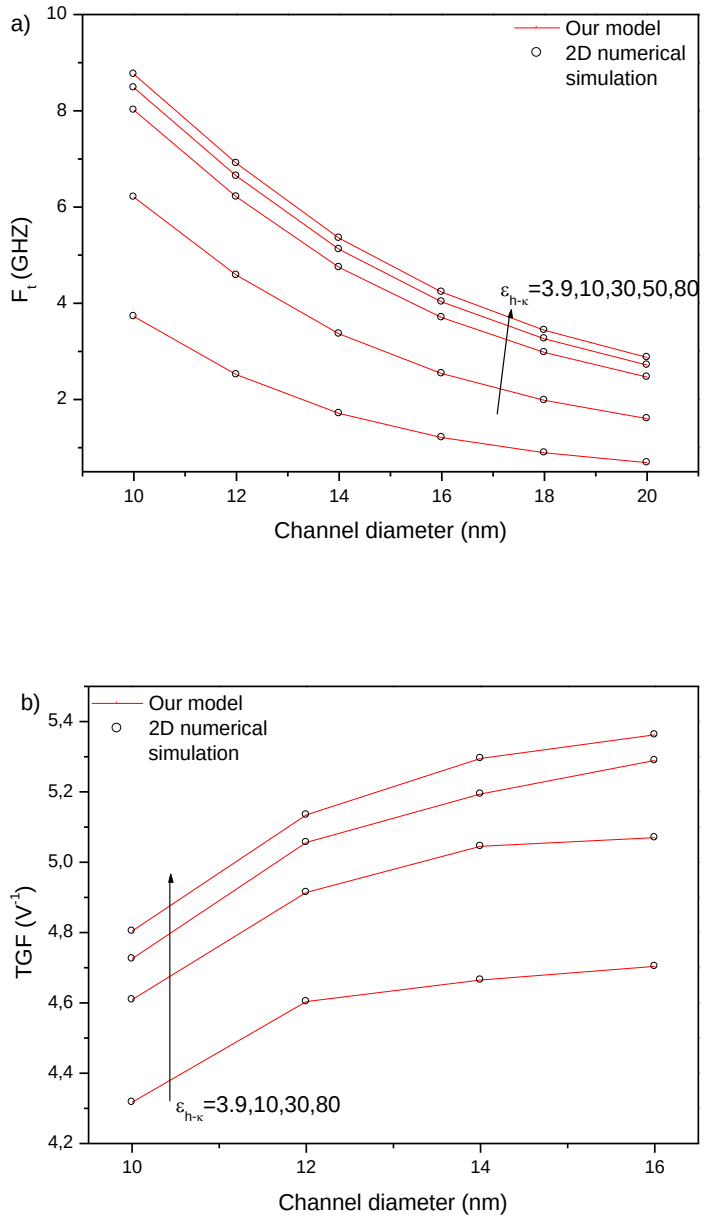

Figure 3.9 – (a) Cut-off frequency as a function of the channel diameter (V_{ds}=1 V and V_{gs}= 1 V) (b) Transconductance generation factor as a function of the channel diameter (V_{ds}=1 V and G_m=0.4 µS).

As a consequence of the transconductance enhancement, the unity gain cut-off frequency is improved in the same way as shown on fig 3.9a. It is expressed as $f_t \approx G_m/(2\pi C_{gg})$ where $C_{gg} = C_{gs} + C_{gd}$ represents the total gate capacitance extracted numerically.

The transconductance generation factor, expressed by $TGF = G_m/I_d$, is another important criterion for analog/RF application which plays a vital role in the field of RF circuit design [34]. It can be interpreted as the efficiency of the device to convert current or implicitly power into transconductance and therefore gain and frequency [35]. To evaluate the effect of the gate stack and radius on TGF, it is extracted at a constant transconductance as shown in fig 3.9b. So, it seems that the TGF drops with the reduction of the channel thickness. However, this degradation is largely compensated by the reduction of the effective oxide thickness.

3.3.2. Linearity analysis

As for MOSFETs, nonlinearity is an inherent TFET characteristic. In analog/RF applications as in low noise amplifier (LNA) or filters, linearity operation range must be determined in order to preserve circuit performance. Due to high second and third order transconductance derivatives, gain compression, distortion and inter modulation become important leading to a signal corruption and a loss of output power [36]. In a nonlinear system, the output can be expressed in a Taylor series expansion as a function of AC gate voltage as [37]:

$$I_{ds} = I_0 + \sum_{i=1} \frac{g_{mi}}{i!} v_{gs}^i \qquad (3.17)$$

where I_0 is DC current component and $g_{mi} = \frac{\partial^i I_{ds}}{\partial v_{gs}^i}$ is i^{th} order of the drain current derivative. From the previous expression, the linearity FOMs can be extracted as [44]:

$$VIP_2 = \frac{4g_{m1}}{g_{m2}} \qquad (3.18.a)$$

$$VIP_3 = \sqrt{\frac{24g_{m1}}{g_{m3}}} \qquad (3.18.b)$$

$$IIP_3 = \frac{4g_{m1}}{R_s g_{m3}} \qquad (3.18.c)$$

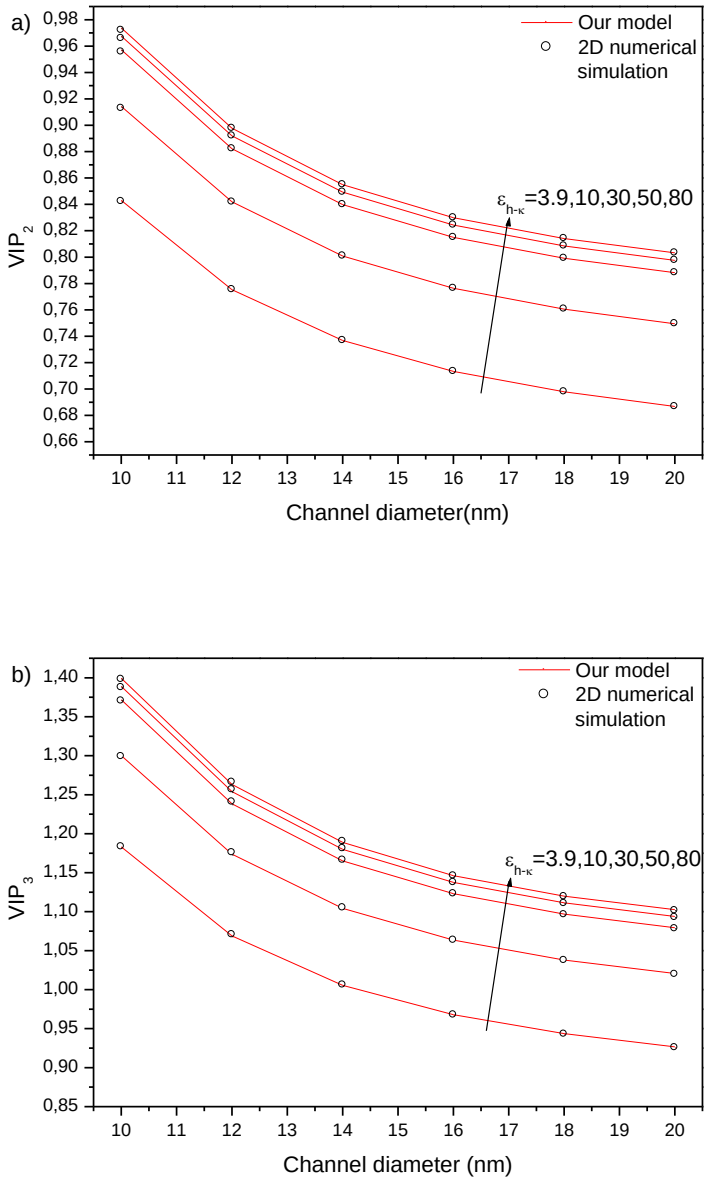

Figure 3.10 – (a) Second order voltage intercept point and (b) Third order voltage intercept point as a function of channel diameter (V_{ds}=1 V and V_{gs}=1 V).

The 2nd and 3rd voltage intercept points denoted respectively by VIP_2 and VIP_3, represent the voltage at which the 2nd and 3rd harmonics reach the fundamental tone and determine the amount of signal distortion [38]. Therefore, highest values of these FOMs mean larger linear operating range. Ideally, in an odd symmetry system, harmonics of even order vanish while in real circuit, symmetry corruption yields to finite number of even order harmonics [36]. As illustrated in fig 3.10, reducing the channel width and the effective oxide thickness enlarges the linear operating range. For two tones input, additional components are generated from the frequencies difference and these non-harmonic components generation phenomena is called intermodulation (IM). In analogy with VIP_3, the 3rd order intermodulation intercept point IIP_3 represents the input at which the 3rd order IM generated components amplitude equals the fundamentals [36, 39]. In the case of a differential LNA, the extrapolated voltage input ($\sqrt{8g_{m1}/g_{m3}}$) is squared and divided by twice the ideal input resistance R_s of 50 Ω to yield IIP_3 in terms of power [40]. As for the previous FOMs, IIP_3 depicted in fig 3.11.a exhibits the same improvement trend.

Even if the increase of the signal amplitude worsens the distortion, the second and the third harmonics can be fortunately filtered, which is not the case for the total fundamental amplitude where the negative second term rising yields to signal compression [39, 40]. This term is generated by the third harmonic and is generally neglected for very small signals. Its effect for higher amplitudes can be extrapolated by means of the 1-dB compression point defined as the input at which the fundamental amplitude drops by 1 dB. It is expressed as $0.38\sqrt{\left|6g_{m1}/g_{m3}\right|}$ for one tone input and $0.22\sqrt{\left|6g_{m1}/g_{m3}\right|}$ for two tones input of the same amplitude [36, 39]. It can be noticed that g_{m3} becomes negative above the threshold voltage and during the drain modulation. As it can be observed in fig 3.6a, computed results for the modeled current derivatives reflect an important error for high V_{gs}. Thus, a more accurate expression of the exponential term describing the drain modulation as $\exp\left(V_{cn}\left(1-\left(\frac{V_c}{V_g^*}\right)^{V'_{cn}}\right)\right)$ is used. Fig 3.11b illustrates the 1-dB compression point input power extracted for both one and two tones respectively in the case of a single-ended LNA and a differential LNA for a 50 Ω input resistance at 1.8 V DC gate bias. It is shown that by reducing

either the channel diameter or the effective oxide thickness the 1-dB compression point is lowered and reduces in turn the dynamic operating range.

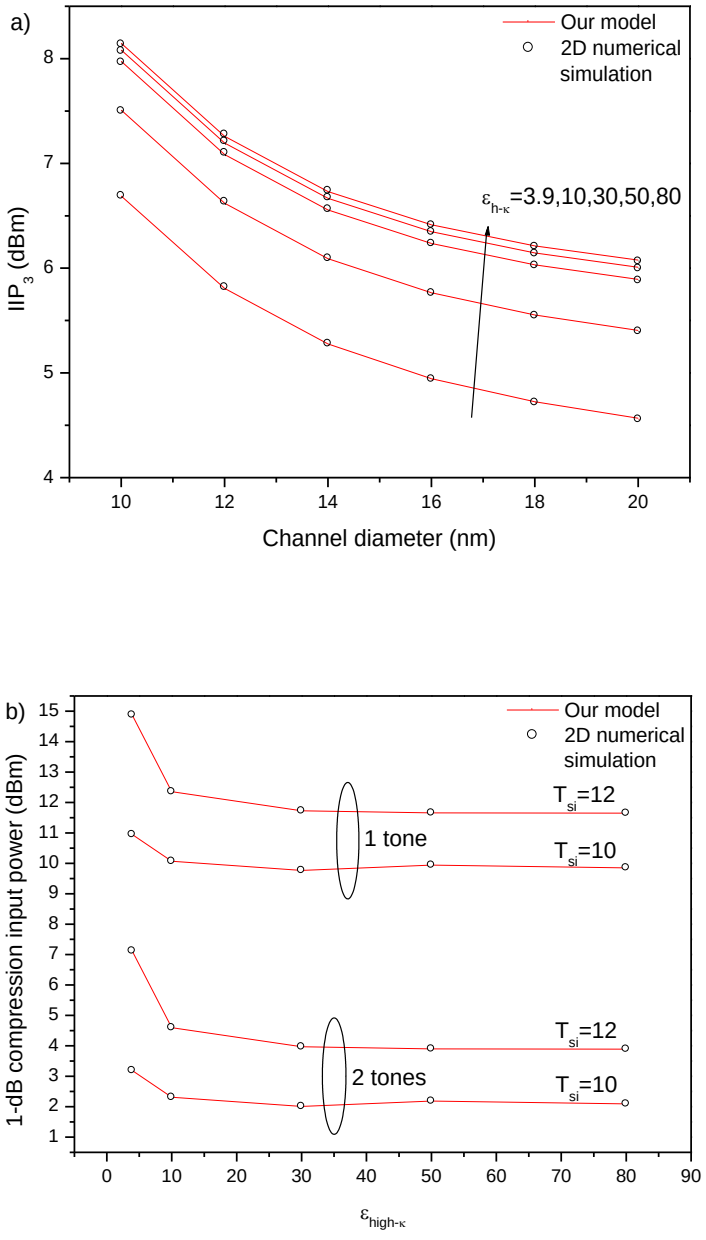

Figure 3.11 – (a) Third order input power intermodulation intercept point as a function of the channel diameter (V_{ds}=1 V and V_{gs}=1 V). (b) 1-dB compression point as a function of the high-κ dielectric constant for (V_{ds}=1 V, V_{gs}=1.8 V).

3.4. Conclusion

In this chapter, a continuous, accurate tunneling current model based on a cylindrical harmonics solution of the 2-D potential was developed for a vertical surrounding-gate structure. The model describes the ambipolar tunneling and dual modulation effects remarkably well. The continuity and high transfer characteristic permit evaluation of device scaling capability, analog/RF performance, and linearity. The results show that decreasing either the channel diameter or effective oxide thickness improves the current and the majority of device FOMs. Moreover, the role of introducing a high-κ layer on the gate oxide in improving the behavior of the VSG-TFET is investigated for use in high-performance analog/RF applications, revealing strong effects on the power consumption and dynamic operating range. Thus, the dimensions and operating supply range should be carefully chosen depending upon the device application. Overall, the results demonstrate a comfortable upper limit of the dynamic operating range with high gain and acceptable cutoff frequency, making such TFET structures promising candidates for use in low-power analog/RF applications.

References

[1] International Technology Roadmap for Semiconductors (ITRS), published online at: http://itrs.net, 2013.

[2] Q. Chen and J. D. Meindl, “Nanoscale metal oxide semiconductor field effect transistors: Scaling limits and opportunities,” Nanotechnology, vol. 15, pp. 8549–8555, Oct. 2004.

[3] T. Bentrcia, F. Djeffal, A. Benhaya, “Continuous analytic I-V model for GS DG MOSFETs including hot-carrier degradation effects,” Journal of Semiconductors, vol. 33, pp. 14001-14006, Jan. 2012.

[4] F. Djeffal, H. Ferhati, T. Bentrcia, “Improved analog and RF performances of gate-all-around junctionless MOSFET with drain and source extensions,” Superlattices and Microstructures, vol. 90, pp. 132-140, Feb. 2016.

[5] ITRS Summer Meeting, Palo Alto, CA, July 11-12, 2015.

[6] G. V. Luong, *et al*., “Complementary Strained Si GAA Nanowire TFET Inverter With Suppressed Ambipolarity,” IEEE Electron Device Letters, vol. 37, pp. 950-953, Aug. 2016.

[7] C. Schulte-Braucks, *et al*., “Experimental demonstration of improved analog device performance of nanowire-TFETs,” Solid-State Electronics, vol. 113, pp. 179-183, Nov. 2015.

[8] S. Datta, H. Liu, V. Narayanan, “Tunnel FET technology: A reliability perspective,” Microelectronics Reliability, vol. 54, pp. 861-874, May. 2014.

[9] A. C. Seabaugh, Q. Zhang, “Low-Voltage Tunnel Transistors for Beyond CMOS Logic,” Proceedings of the IEEE, vol. 98, pp. 2095-2110, Dec. 2010.

[10] M. G. Bardon, H. P. Neves, R. Puers, C. V. Hoof, “Pseudo-Two-Dimensional Model for Double-Gate Tunnel FETs Considering the Junctions Depletion Regions,” IEEE Transactions on Electron Devices, vol. 57, pp. 827-834, Apr. 2010.

[11] L. Zhang, X. Lin, J. He, M. Chan, “An Analytical Charge Model for Double-Gate Tunnel FETs,” IEEE Transactions on Electron Devices, vol. 59, pp. 3217-3223, Dec. 2012.

[12] C. Shen, *et al*., “A Variational Approach to the Two-Dimensional Nonlinear Poisson’s Equation for the Modeling of Tunneling Transistors,” IEEE Transactions on Electron Devices, vol. 29, pp. 1252-1255, Nov. 2008.

[13] A. Pan, S. Chen, C. On Chui, “Electrostatic Modeling and Insights Regarding Multigate Lateral Tunneling Transistors,” IEEE Transactions on Electron Devices, vol. 60, pp. 2712-2720, Sep. 2013.

[14] P. A. Patel, “Steep Turn On/Off "Green" Tunnel Transistors,” PhD dissertation, University of California, Berkeley,2010.

[15] L. Zhang, M. Chan, “SPICE Modeling of Double-Gate Tunnel-FETs Including Channel Transports,” IEEE Transactions on Electron Devices, vol. 61, pp. 300-307, Feb. 2014.

[16] A. Pal, A. K. Dutta, “Analytical Drain Current Modeling of Double-Gate Tunnel Field-Effect Transistors,” IEEE Transactions on Electron Devices, vol. 63, pp. 3213-3221, Aug. 2016.

[17] J. Min, J. Wu, Y. Taur, “Analysis of Source Doping Effect in Tunnel FETs With Staggered Bandgap,” IEEE Electron Device Letters, vol. 36, pp. 1094-1096, Oct. 2015.

[18] Y. Taur, J. Wu, J. Min, “An Analytic Model for Heterojunction Tunnel FETs With Exponential Barrier,” IEEE Transactions on Electron Devices, vol. 62, pp. 1399-1404, May. 2015.

[19] H. R. Tajik Khaveh, S. Mohammadi, “Potential and Drain Current Modeling of Gate-All-Around Tunnel FETs Considering the Junctions Depletion Regions and the Channel Mobile Charge Carriers,” IEEE Transactions on Electron Devices, vol. 63, pp. 5021-5029, Dec. 2016.

[20] M. Gholizadeh, S. E. Hosseini, “A 2-D Analytical Model for Double-Gate Tunnel FETs,” IEEE Transactions on Electron Devices, vol. 61, pp. 1494-1500, May. 2014.

[21] ATLAS User Manual: Device Simulation Software, 2012.

[22] C. Wu, R. Huang, Q. Huang, “An Analytical Surface Potential Model Accounting for the Dual-Modulation Effects in Tunnel FETs,” IEEE Transactions on Electron Devices, vol. 61, pp. 2690-2696, Aug. 2014.

[23] N. D. Chien, C. H. Shih, “Short channel effects in tunnel field-effect transistors with different configurations of abrupt and graded Si/SiGe heterojunctions,” Superlattices and Microstructures, vol. 100, pp. 857-866, Dec. 2016.

[24] H. Abd El Hamid, B. Iñíguez, J. R. Guitart, “Analytical Model of the Threshold Voltage and Subthreshold Swing of Undoped Cylindrical Gate-All-Around-Based MOSFETs,” IEEE Transactions on Electron Devices, vol. 54, pp. 572-579, Mar. 2007.

[25] P. L. Chambré, “On the Solution of the Poisson-Boltzmann Equation with Application to the Theory of Thermal Explosions,” The Journal of Chemical Physics, vol. 20, pp. 1795-1797, Nov. 1952.

[26] A. D. Polyanin, “Handbook of Linear Partial Differential Equation for Engineers and Scientists,” Chapman & Hall/CRC, 2002.

[27] N. H. Asmar, “Partial Differential Equations with Fourier Series and Boundary Value Problems,” Pearson Prentice Hall, 2004.

[28] B. Ray, S. Mahapatra, “Modeling and Analysis of Body Potential of Cylindrical Gate-All-Around Nanowire Transistor,” IEEE Transactions on Electron Devices, vol. 55, pp. 2409-2416, Sep. 2008.

[29] D. B. Abdi, M. J. Kumar, “2-D Threshold Voltage Model for the Double-Gate p-n-p-n TFET With Localized Charges,” IEEE Transactions on Electron Devices, vol. 63, pp. 3663-3668, Jul. 2016.

[30] E. O. Kane, “Zener tunneling in semiconductors,” Journal of Physics and Chemistry of Solids, vol. 12, pp. 181-188, Jan. 1960.

[31] L. Liu, D. Mohata, S. Datta, “Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors,” IEEE Transactions on Electron Devices, vol. 59, pp. 902-908, Apr. 2012.

[32] S. M. Biswal, B. Baral, D. De, A. Sarkar, “Study of effect of gate-length downscaling on the analog/RF performance and linearity investigation of InAs-based nanowire Tunnel FET,” Superlattices and Microstructures, vol. 91, pp. 319-330, Mar. 2016.

[33] D. Rechem, A. Khial, C. Azizi, F. Djeffal, “Impacts of high-k gate dielectrics and low temperature on the performance of nanoscale CNTFETs,” Journal of Computational Electronics, vol. 15, pp. 1308-1315, Dec. 2016.

[34] G. Cornetta, D. J. Santos, J. M. Vazquez, “Wireless Radio-Frequency Standards and System Design: Advanced Techniques 1st edition,” IGI Publishing Hershey, USA, 2012.

[35] R. K. Baruah, R. P. Paily, “A Dual Material Double-Layer Gate Stack Junctionless Transistor for Enhanced Analog Performance,” VLSI Design and Test 17th International Symposium, VDAT 2013, Jaipur, India, July 27-30, 2013.

[36] B. Razavi, “RF Microelectronics,” Prentice Hall, USA, 1998.

[37] W. Ma, S. Kaya, “Impact of device physics on DG and SOI MOSFET linearity,” Solid-State Electronics, vol. 48, pp. 1741-1746, Oct–Nov. 2004.

[38]T. Bentrcia, F. Djeffal, E. Chebaki and D. Arar, “Impact of the drain and source extensions on nanoscale Double-Gate Junctionless MOSFET analog and RF performances,” Materials Science in Semiconductor Processing, vol. 42, pp. 264-267, Feb. 2016.

[39] J. Rogers, C. Plett, “Radio Frequency Integrated Circuit Design,” Artech House, USA, 2003.

[40] T. H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits,” Second edition, Cambridge University Press, 2004.

CHAPTER 4:

Semi-analytical modeling of the heterojunction VSG TFET

4.1. Introduction

Over the past decade, III-V materials and heterostructure are gaining attention as TFETs performances booster. The heterostructure advantage was demonstrated in many experimental and simulation studies [1-4]. The material composition, especially ternary compounds, that offers large flexibility in the physical properties variation such as bandgap, carriers' effective masses and band alignment type yields tremendous possibilities to enhance the device performances either high performance or low power specifications are targeted. Indeed, record on-current and subthreshold slope were experimentally obtained for different III-V heterostructure TFETs [5]. The source doping impact on the subthreshold slope was previously highlighted and suggests the existence of an optimal doping that offers the best compromise between the off- and on-state characteristics [6]. Therefore, heterostructure TFETs need more attention and deeper investigation on the device physics and performances for an efficient improvement. For this aim, it is necessary to develop accurate models that facilitate such task.

The modeling of heterostuctrure TFETs implies the use of nonlocal tunneling model as the constant electric field assumption is no longer applicable to the heterojunction. Therefore, reliable tunneling current evaluation should be based on self-consistent solution of the Poisson equation to accurately reproduce the electrostatic distribution. This necessity is also justified by the fact that the analytical description of the fringing electric field impact on the source and drain, knowing the importance of this effect on the tunneling junction extensions, is a very difficult task. Furthermore, the electrostatic distribution deformation and the non-equilibrium state induced by the high tunneling current injection and the resulting charge dipole creation becomes cumbersome. Also, the inclusion of the Schrödinger equation in the simulation scheme permits a precise evaluation of the tunneling and quantum transport. Therefore, the study of heterostructure TFETs either with commercial simulators or developed ones based on NEGF as in [3], is certainly a more reliable solution but highly time consuming. Moreover, the use of such tools for large circuits simulation or for optimization purpose is further complicated and might require the employing of look-up tables [7].

On the other hand, the feasibility of heterostructure TFET analytical modeling was previously studied [4, 8, 9]. The basis of this approach consists on the evaluation of the tunneling probability of each material separately; their sum yields the total probability. If this approach is physically incorrect, it gives nonetheless acceptable quantitative description of the tunneling probability evolution [4, 9]. Furthermore, the exponential barrier assumption that applies to long channels simplifies the integral of the imaginary wavevector and yields analytical expressions of the tunneling probability [8, 9]. Nevertheless, the precedent studies settle for the evaluation of the tunneling probability or limit the current computation to the source junction. Moreover, the depletion approximation applied to the source potential is unreliable.

In this chapter, a semi-analytical model of heterostructure VSG TFET is presented. This model is valid for a wide range of device dimensions, materials and supplies. The drain modulation is also described as well as the ambipolar current which is essential to a reliable assessment of the device performances. The electrostatic distribution is solved using the exponential approximation which is consistent with the cylindrical harmonics solution developed in the previous chapter. A good estimation of the junctions' boundary potentials is performed using both Fermi-Dirac and Boltzmann statistics. Furthermore, the conformal transformation is used to obtain the extensions potential profile. The heterostructure band alignment is calculated using the affinity rule. Applying nonlocal tunneling model and the WKB approximation, the proposed model yields encouraging results in both quantitative and qualitative aspect. Respectively, the model is calibrated and validated by 2-D numerical simulations [10]. An analysis of the device material choice, doping and dimensions impact on the device characteristics is also performed. Besides, terminals' capacitances expressions are derived. Finally, by employing the multi-objective genetic paradigm, the optimization of the device performances for both digital and analog application is carried out.

4.2. Electrostatic model derivation

In the following study, a vertical surrounding gate structure is considered as exposed in fig 4.1a. The developed model is valid for a wide range of dimensions and material parameters. The channel length however is limited to 100 nm and thus to avoid SCEs and

direct source to drain tunneling. The source doping varies between 10^{20} and 10^{19} cm^{-3} while the drain doping is fixed to 10^{19} cm^{-3} to ensure ohmic contacts formation and avoid further current limitation.

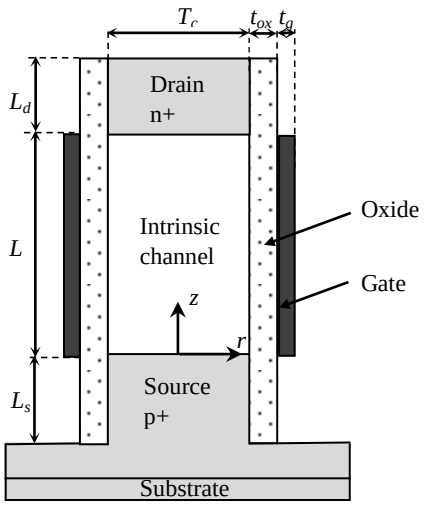

Figure 4.1a – Cross sectional view of the vertical surrounding gate heterojunction TFET structure.

Because the present tunneling model is based on nonlocal approach, it is primordial to develop an accurate potential profile in the whole structure. As exposed in the previous chapter, the channel electrostatic solution includes two components, the 1D Poisson equation solution, denoted by $V_c(r)$ which is obtained using (3.4) and the 2-D component which is simplified from cylindrical harmonic solution to an exponential based expression valid for long channels. The final channel potential can be written as:

$$\psi(r,z) = V_c(r) + \left(V_{ps}(r) - V_c(r)\right)\exp\left(-\lambda_c z\right) + \left(V_{pd}(r) - V_c(r)\right)\exp\left(\lambda_c z\right)/\left(2\sinh(\lambda_c L)\right) \quad (4.1)$$

with $\lambda_c = (3/\pi)^{1/4}\lambda\exp\left(1 - V_c / V_{gc}^*\right)$

where λ represents the inverse of the classical scaling length obtained from the pseudo-2-D solution of the Poisson equation and is defined as $\lambda = \sqrt{2C/a}$ with $C = C_{ox}/\varepsilon_c$, C_{ox} and ε_c being the oxide capacitance and channel material permittivity respectively [11, 12]. The pre-factor was found from simulations and permits to compensate the impact of the lateral electric fields near the junctions [13]. Also, the exponential term accounts for the drain modulation effect as introduced in the precedent chapter. V_{ps} and V_{pd} are respectively the

source and drain junctions' potentials. These latter are controlled by the depletion effect induced by both channel and gate potentials. For their extraction, the following drain/source Poisson equation is considered:

$$\frac{\partial^2\psi_{s,d}(r,z)}{\partial z^2}+\frac{1}{r}\frac{\partial\psi_{s,d}(r,z)}{\partial r}+\frac{\partial^2\psi_{s,d}(r,z)}{\partial r^2}=-\frac{q}{\varepsilon_{s,d}}\rho_{s,d}(r,z) \tag{4.2}$$

Assuming a parabolic potential profile in the radial direction, the perpendicular electric field at r=0 tends toward zero, thus the Poisson equation can be set as:

$$\frac{\partial^2\psi_s(0,z)}{\partial z^2}=\frac{q}{\varepsilon_S}\left(N_{AS}-N_{vs}F_{1/2}\left(\frac{-\psi_s(0,z)-E_{is}-E_{fp}}{V_t}\right)\right) \tag{4.3.1}$$

with $E_{is}=\frac{E_{gs}}{2}+\frac{V_t}{2}\log\left(\frac{N_{vs}}{N_{cs}}\right)$

$$\frac{\partial^2\psi_s(0,z)}{\partial z^2}=\frac{q}{\varepsilon_S}\left(N_{AS}-n_{is}\exp\left(\frac{-\psi_s(0,z)+V_{fp}}{V_t}\right)\right) \tag{4.3.2}$$

where ψ_s, ε_s, N_{AS}, N_{vs}, N_{cs}, n_{is}, E_{gs}, E_{is}, E_{fp}, V_{fp} are the source potential, permittivity, doping, hole and electron density of states, intrinsic carrier concentration, bandgap, intrinsic Fermi level, hole quasi Fermi level and its corresponding potential, respectively. Here, Fermi-Dirac statistics are considered in the aim of obtaining a more realistic behavior of heavily doped tunneling junctions. If the Boltzmann statistics are preferred, expression (4.3.2) is used. $F_{1/2}$ represents the complete Fermi-Dirac integral of order 1/2. It is also noticed that the energies are expressed in Volts for simplification. Analogous, the drain side Poisson equation takes the form:

$$\frac{\partial^2\psi_d(0,z)}{\partial z^2}=\frac{q}{\varepsilon_d}\left(-N_{DD}+N_{cd}F_{1/2}\left(\frac{\psi_d(0,z)+E_{id}-E_{gd}+E_{fn}}{V_t}\right)\right) \tag{4.4.1}$$

with $E_{id}=\frac{E_{gd}}{2}+\frac{V_t}{2}\log\left(\frac{N_{vd}}{N_{cd}}\right)$

$$\frac{\partial^2\psi_d(0,z)}{\partial z^2}=\frac{q}{\varepsilon_d}\left(-N_{DD}+n_{id}\exp\left(\frac{\psi_d(0,z)-V_{fn}}{V_t}\right)\right) \tag{4.4.2}$$

where the parameters definitions being equivalent to the source side. Assuming a zero lateral electric field at the source and drain contacts, the junctions' potentials at the body center can be obtained by the method proposed in [14], i.e. multiplying both sides of the precedent expressions by $\partial\psi/\partial z$ and integrating once with respect to the potential yielding:

$$\int_{L_s}^{0} \frac{\partial^2 \psi_s(0,z)}{\partial z^2} \frac{\partial \psi_s(0,z)}{\partial z} = \int_{L_s}^{0} \frac{q}{\varepsilon_s} \left(N_{AS} - N_{vs} F_{1/2}\left(\frac{-\psi_s(0,z) - E_{is} - E_{fp}}{V_t} \right) \right) \frac{\partial \psi_s(0,z)}{\partial z}$$

$$\int_{0}^{E_{\perp ps}(0)} E_s \partial E_s = \int_{V_{bis}}^{V_{ps}(0)} \frac{q}{\varepsilon_s} \left(N_{AS} - N_{vs} F_{1/2}\left(\frac{-\psi_s(0,z) - E_{is} - E_{fp}}{V_t} \right) \right) \partial \psi_s$$

$$\frac{E_{\perp ps}(0)}{\sqrt{2}} = \operatorname{sgn}\left(V_{ps}(0) - V_{bis}\right) \sqrt{\frac{q}{\varepsilon_S} \left| \begin{array}{l} N_{AS}\left(V_{ps}(0) - V_{bis}\right) \\ -V_t N_{vs} \left(F_{3/2}\left(\frac{-V_{ps}(0) - E_{is} - E_{fp}}{V_t} \right) - F_{3/2}\left(\frac{-V_{bis} - E_{is} - E_{fp}}{V_t} \right) \right) \end{array} \right|}$$

(4.5)

Similarly to the source side, the drain Poisson equation can be rewritten as:

$$\int_{L}^{L_d} \frac{\partial^2 \psi_d(0,z)}{\partial z^2} \frac{\partial \psi_d(0,z)}{\partial z} = \int_{L}^{L_d} \frac{q}{\varepsilon_d} \left(-N_{DD} + N_{cd} F_{1/2}\left(\frac{\psi_d(0,z) + E_{id} - E_{gd} + E_{fn}}{V_t} \right) \right) \frac{\partial \psi_d(0,z)}{\partial z}$$

$$\int_{E_{\perp pd}(0)}^{0} E_d \partial E_d = \int_{V_{pd}}^{V_{bid}} \frac{q}{\varepsilon_d} \left(-N_{DD} + N_{cd} F_{1/2}\left(\frac{\psi_d(0,z) + E_{id} - E_{gd} + E_{fn}}{V_t} \right) \right) \partial \psi_d$$

$$\frac{E_{\perp pd}(0)}{\sqrt{2}} = \operatorname{sgn}\left(V_{bid} - V_{pd}(0)\right) \sqrt{\frac{q}{\varepsilon_d} \left| \begin{array}{l} -N_{DD}\left(V_{bid} - V_{pd}(0)\right) \\ +V_t N_{cd} \left(F_{3/2}\left(\frac{V_{bid} + E_{id} - E_{gd} + E_{fn}}{V_t} \right) - F_{3/2}\left(\frac{V_{pd}(0) + E_{id} - E_{gd} + E_{fn}}{V_t} \right) \right) \end{array} \right|}$$

(4.6)

The electric field continuity at the junctions implies that $E_{\perp ps}(0) = \lambda_c \left(V_{ps}(0) - V_c(0)\right)$ and $E_{\perp pd}(0) = -\lambda_c \left(V_{pd}(0) - V_c(0)\right)$. Finally, the boundary potentials solutions have to be computed numerically. Following the same approach, the equivalent equations based on the Boltzmann statistics can be expressed as:

$$\frac{E_{\square ps}(0)}{\sqrt{2}} = \operatorname{sgn}\left(V_{ps}(0) - V_{bis}\right)\sqrt{\frac{q}{\varepsilon_S}\left|N_{AS}\left(V_{ps}(0) - V_{bis}\right) - V_t n_{is}\left(\exp\left(\frac{-V_{ps}(0) + V_{fp}}{V_t}\right) - \exp\left(\frac{-V_{bis} + V_{fp}}{V_t}\right)\right)\right|}$$

(4.7)

$$\frac{E_{\square pd}(0)}{\sqrt{2}} = \operatorname{sgn}\left(V_{bid} - V_{pd}(0)\right)\sqrt{\frac{q}{\varepsilon_d}\left|-N_{DD}\left(V_{bid} - V_{pd}(0)\right) + V_t n_{id}\left(\exp\left(\frac{V_{bid} - V_{fn}}{V_t}\right) - \exp\left(\frac{V_{pd}(0) - V_{fn}}{V_t}\right)\right)\right|}$$

(4.8)

with V_{bis} and V_{bid} represent the source and drain potentials at the contacts composed of the built-in potentials and the quasi Fermi levels. These potentials can be obtained by solving the following expressions:

$$N_{vs} F_{1/2}\left(\frac{-V_{bis} - E_{is} - E_{fp}}{V_t}\right) = N_{AS} \tag{4.9}$$

$$N_{cd} F_{1/2}\left(\frac{V_{bid} + E_{id} - E_{gd} + E_{fn}}{V_t}\right) = N_{DD} \tag{4.10}$$

For the Boltzmann statistics, the previous definitions can be simplified as:

$$V_{bis} = -V_t \log\left(N_{AS}/n_{is}\right) + V_{fp} \tag{4.11}$$

$$V_{bid} = V_t \log\left(N_{DD}/n_{id}\right) + V_{fn} \tag{4.12}$$

The next step is to extract the junctions' potentials at the surface. This can be achieved by following the precedent procedure in the radial direction this time. Therefore, the Poisson equation of the two junctions for both statistics types gives:

$$E_{\perp ps}(a) = \operatorname{sgn}\left(V_{ps}(a) - V_{ps}(0)\right)\sqrt{\frac{q}{\varepsilon_S}\left|\begin{array}{l} N_{AS}\left(V_{ps}(a) - V_{ps}(0)\right) \\ -V_t N_{vs}\left(F_{3/2}\left(\frac{-V_{ps}(a) - E_{is} - E_{fp}}{V_t}\right) - F_{3/2}\left(\frac{-V_{ps}(0) - E_{is} - E_{fp}}{V_t}\right)\right)\end{array}\right|}$$

(4.13)

$$E_{\perp pd}(a) = \operatorname{sgn}\left(V_{pd}(a) - V_{pd}(0)\right)\sqrt{\frac{q}{\varepsilon_d}\left|\begin{array}{l} -N_{DD}\left(V_{pd}(a) - V_{pd}(0)\right) \\ +V_t N_{cd}\left(F_{3/2}\left(\frac{V_{pd}(a) + E_{id} - E_{gd} + E_{fn}}{V_t}\right) - F_{3/2}\left(\frac{V_{pd}(0) + E_{id} - E_{gd} + E_{fn}}{V_t}\right)\right)\end{array}\right|}$$

(4.14)

$$E_{\perp ps}(a)=\operatorname{sgn}\left(V_{ps}(a)-V_{ps}(0)\right)\sqrt{\frac{q}{\varepsilon_S}\left|\begin{array}{l}N_{AS}\left(V_{ps}(a)-V_{ps}(0)\right)\\-V_t n_{is}\left(\exp\left(\frac{-V_{ps}(a)+V_{fp}}{V_t}\right)-\exp\left(\frac{-V_{ps}(0)+V_{fp}}{V_t}\right)\right)\end{array}\right|}$$

(4.15)

$$E_{\perp pd}(a)=\operatorname{sgn}\left(V_{pd}(a)-V_{pd}(0)\right)\sqrt{\frac{q}{\varepsilon_d}\left|\begin{array}{l}-N_{DD}\left(V_{pd}(a)-V_{pd}(0)\right)\\+V_t n_{id}\left(\exp\left(\frac{V_{pd}(a)-V_{fn}}{V_t}\right)-\exp\left(\frac{V_{pd}(0)-V_{fn}}{V_t}\right)\right)\end{array}\right|}$$

(4.16)

Here the perpendicular electric field satisfies the continuity conditions at the channel/oxide and junctions' interfaces i.e. $\left.\frac{\partial\psi_c}{\partial r}\right|_{r=a}=\frac{C_{ox}}{\varepsilon_c}\left(V_g^*-\psi(a,z)\right)$ and $\left.\frac{\partial\psi_{s,d}}{\partial r}\right|_{\substack{r=a\\z=0,L}}=\left.\frac{\partial\psi_c}{\partial r}\right|_{\substack{r=a\\z=0,L}}$ which gives $E_{\perp ps,d}(a)=\frac{C_{ox}}{\varepsilon_c}\left(V_g^*-V_{ps,d}(a)\right)$.

V_g^* is the effective gate voltage defined as $V_g^*=V_g-V_{fb}$ with $V_{fbc}=\Phi_m-\chi_c-E_{gc}+E_{ic}$ being the flat band voltage where Φ_m, χ_c represent the gate work function and channel electron affinity, respectively. The next step is to model the electrostatic profile of the extensions, or at least its surface potential. The extensions potential can be evaluated using a pseudo-2-D solution of the Poisson equation such as [11]:

$$\psi_{s,d}(r,z)=C_0(z)+C_1(z)(r-a)+C_2(z)(r-a)^2 \qquad (4.18)$$

which transforms the Poisson equation with the right boundary conditions to:

$$\frac{\partial^2\psi_{s,d}(a,z)}{\partial z^2}+\frac{2C_{ox}(z)\left(V^*_{g(s,d)}-\psi_{s,d}(z,a)\right)}{a\varepsilon_{s,d}}=-\frac{q}{\varepsilon_{s,d}}\rho_{s,d}(a,z) \qquad (4.19)$$

The main difficulty in the resolution of this equation is the consideration of the gate electrode fringing fields that yields a variable oxide capacitance. This problem was previously treated in a simple manner in [11], where a coefficient of $\pi/2$ was introduced in the classical capacitance expression. A more developed analysis was carried out in [15] to produce an analytical surface potential expression using the conformal mapping technique.

Performing a similar approach as in [16, 17], a conformal transformation of the electric field lines into oxide region is introduced as illustrated in fig 4.1b. With the appropriate transformation function $w=\sin(z)$, the coordinates can be mapped as follows:

$$(r-a)\vec{R}+Nz\vec{Z}=t_{ox}\sin\left(u\vec{U}+v\vec{V}\right) \tag{4.20}$$

with $N_{s,d}=\dfrac{-t_{ox}}{L_{s,d}}\sinh\left(\cosh^{-1}\left(\dfrac{t_{ox}+t_g}{t_{ox}}\right)\right)$

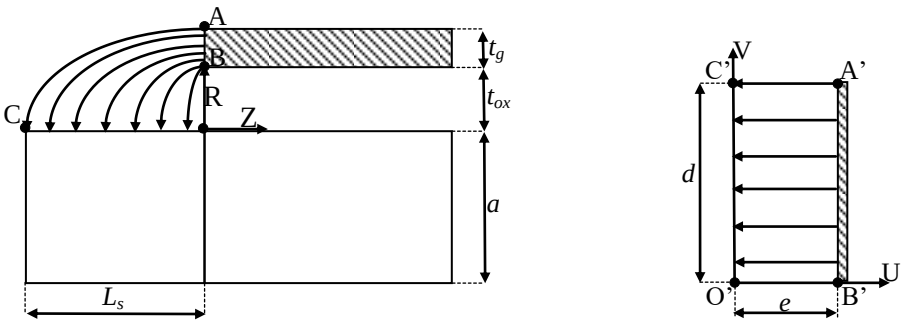

Figure 4.1b – Illustration of the fringing electric field lines in the original coordinates (left) and the transformed representation (right).

The expression of the original coordinates axis as a function of the transformed ones gives $z=\dfrac{t_{ox}}{N_{s,d}}\sinh(v)$ for $r=a$ and $r-a=t_{ox}\sin(u)$ for $z=0$. Accordingly, the transformation of the extensions lengths and oxide thickness yields $d_{s,d}=\sinh^{-1}\left(\dfrac{-N_{s,d}L_{s,d}}{t_{ox}}\right)$ and $e=\dfrac{(1+2n)\pi}{2}$.

Applying these transformed dimensions, the oxide capacitance in the new coordinate system takes the form:

$$C_{oxs,d}=\frac{\varepsilon_{s,d}}{a'_{s,d}\log\left(1+\dfrac{e}{a'_{s,d}}\right)} \qquad \text{where} \quad a'_{s,d}=\sinh^{-1}\left(\frac{aN_{s,d}}{t_{ox}}\right) \tag{4.21}$$

A correct conformal representation has some implications. The first one is that Laplace's equation takes the same form as the original coordinates. By extensions, this implication is also valid for Poisson's equation with the introduction of a scale factor that gives to the transformed variables *u* and *v* physical lengths as these latter are unitless [17]. The second implication of the conformal representation is that $\frac{\partial v}{\partial z}=\frac{\partial u}{\partial r}$. Knowing from the axis transformation that $\partial z=\frac{N_{s,d}}{t_{ox}}\cosh(v)\partial v$, the scale factor is then $\frac{N_{s,d}}{t_{ox}}\cosh(v)$. Consequently, the Poisson equation in the new coordinates can be rewritten as:

$$\left(\frac{N_{s,d}}{t_{ox}\cosh(v)}\right)^2\left(\frac{\partial^2\psi_{s,d}(u,v)}{\partial v^2}+\frac{1}{u}\frac{\partial\psi_{s,d}(u,v)}{\partial u}+\frac{\partial^2\psi_{s,d}(u,a)}{\partial u^2}\right)=-\frac{q}{\varepsilon_{s,d}}\rho_{s,d}(u,v) \qquad (4.22)$$

Considering the solution in the vicinity of the junctions' interfaces where $\cosh(v)$ tends toward 1 and neglecting the majority carriers, the Poisson equation can be simplified to:

$$\frac{\partial^2\psi_{s,d}(0,v)}{\partial v^2}+\frac{2C_{oxs,d}\left(V^*_{g(s,d)}-\psi_{s,d}(0,v)\right)}{a'_{s,d}\varepsilon_{s,d}}\approx\pm\left(\frac{t_{ox}}{N_{s,d}}\right)^2\frac{q}{\varepsilon_{s,d}}N_{AS,DD} \qquad (4.23)$$

The oxide capacitance being now constant, the pseudo 2-D solution with the boundary conditions is expressed as:

$$\psi_{s,d}(0,v)=V_{bis,d}+(V_{ps,d}(a)-V_{bis,d})\exp(v/\lambda^*_{s,d}) \qquad (4.24)$$

Replacing *v* by its equivalent in the original coordinates, the surface potential takes the final form:

$$\psi_s(a,z)=V_{bis}+(V_{ps}(a)-V_{bis})\exp\left(\frac{\sinh^{-1}\left(zN_s/t_{ox}\right)}{\lambda^*_s}\right) \qquad (4.25)$$

$$\psi_d(a,z)=V_{bid}+(V_{pd}(a)-V_{bid})\exp\left(\frac{\sinh^{-1}\left((z-L)N_d/t_{ox}\right)}{\lambda^*_d}\right) \qquad (4.26)$$

It is noticed that these expressions differ somehow from what the resolution of (4.23) should give and is obtained by identification. Also, the gate voltage is not explicitly expressed. This information is therefore included in the scaling length. As for λ_c, simulations

highlighted that the extensions scaling lengths show a strong dependence on the gate voltage. Denoted $\lambda_{s,d}^{*}$, it can be obtained from the following expression:

$$\frac{V_{ps,d}(a)-V_{bis,d}}{\alpha\left(\lambda_{s,d}^{*}\right)^{2}}+\frac{V_{g/s,d}^{*}-V_{ps,d}(a)}{\left(\lambda_{s,d}\right)^{2}}=-\frac{q}{\varepsilon_{s,d}}\rho_{s,d}(a)\left(\frac{t_{ox}}{N_{s,d}}\right)^{2} \tag{4.27}$$

where $\lambda_{s,d}=\sqrt{\frac{a'_{s,d}\varepsilon_{s,d}}{2C_{oxs,d}}}$ and $V_{g/s,d}^{*}=V_g-V_{fb/s,d}$. The extensions flat band voltage $V_{fb/s,d}$ are defined by $V_{fb/s,d}=\Phi_m-\chi_{s,d}-E_{gs,d}+E_{is,d}+V_{bis,d}-V_{qn,p}$. It is worth mentioning that the obtained expressions represent an approximated solution that might induce a consequent error on the tunneling current evaluation, especially for moderate doping extensions that yields deeper depletion and more complex potential profile. Therefore, it is necessary to introduce a correction factor. This latter noted α is introduced in denominator of the first term in (4.27) and a value of 3 for both extensions was found to give good results. Furthermore, the use of Boltzmann statistics in the derivation of the channel potential expression (3.4) when Fermi-Dirac statistics are considered in the remaining device regions yields large error during the drain modulation. Thus, a correction is applied to the channel potential as $(V_c+V_g^{*})/2$. Otherwise, a numerical resolution of the 1D Poisson equation should be used.

4.3. Heterostructure band alignment

The band alignment in heterostructure can take three configurations or types, namely straddled-, staggered- and broken-gap. In this work, the affinity rule is used to determine the conduction and valence band discontinuity [18, 10]. The resulting definitions of this rule are:

$$\begin{cases}\Delta E_c=\chi_c-\chi_s\\ \Delta E_g=E_{gs}-E_{gc}\\ \Delta E_v=\Delta E_g-\Delta E_c\\ E_r=E_{gc}-E_{ic}+\chi_c\end{cases} \tag{4.28}$$

E_r is defined as the energy reference from which the band alignment is calculated and refers to the smallest bandgap of the three regions. Overall, in most cases of n-type TFET, E_r corresponds to the channel and drain energy reference as the same material is used for both regions and thus to avoid any possible transport limitation of the heterojunction. In the reverse case where E_{gs}>$E_{gc,d}$, the previous definitions and following development are still valid. As a consequence of the alignment, the extensions' built-in and junctions' potentials are shifted with an amount defined as $\Delta V = E_{is,d} - E_{gs,d} - \chi_{s,d} + E_r$ and the new values are computed by $V^*_{bis,d} = V_{bis,d} + \Delta V$ and $V^*_{ps,d} = V_{ps,d} + \Delta V$. Also, these latter definitions are involved in the calculation of the junctions' potentials and the extensions scaling lengths. The electric fields are then rewritten as $E_{\parallel ps,d}(0) = \lambda_c \left(V_c(0) - V^*_{ps,d}(0) \right)$ and $E_{\perp ps,d}(a) = \frac{C_{ox}}{\varepsilon_c}\left(V^*_g - V^*_{ps,d}(a) \right)$, while the RHS of the concerned equations remains unchanged. Furthermore, equation (4.27) is redefined as:

$$\frac{V^*_{ps,d}(a) - V^*_{bis,d}}{\alpha\left(\lambda^*_{s,d}\right)^2} + \frac{V^*_{g/s,d} - V^*_{ps,d}(a)}{\left(\lambda_{s,d}\right)^2} = -\frac{q}{\varepsilon_{s,d}} \rho_{s,d}(a) \left(\frac{t_{ox}}{N_{s,d}} \right)^2 \tag{4.29}$$

All the necessary parameters being extracted, the valence and conduction bands (E_c= E_v+E_g) definitions in the three regions are:

$$E_{vs} = -V_{bis} - \left(V_{ps}(a) - V_{bis} \right) \exp\left(-\frac{zN_s}{\lambda^*_s t_{ox}} \right) - E_{is} \tag{4.30}$$

$$E_{vc} = -V_c - \left(V^*_{ps}(a) - V_c \right) \exp\left(-\lambda_c z \right) - \left(V^*_{pd}(a) - V_c \right) \exp\left(\lambda_c z \right) / \left(2\sinh\left(\lambda_c L \right) \right) - E_{ic} \tag{4.31}$$

$$E_{vd} = -V_{bid} - \left(V_{pd}(a) - V_{bid} \right) \exp\left(-\frac{(z-L)N_d}{\lambda^*_d t_{ox}} \right) - E_{id} \tag{4.32}$$

The next figures illustrate the heterojunction TFET energy band diagrams for various materials and doping. It is observed that the proposed model offers a good match with the numerical results. As pointed out previously, the main concern is the extensions potential profile for low doping concentrations as it is showcased in fig 4.3. Obviously, the case is more critical as the model may suffer from some anomalies in describing properly the electrostatic profile as a consequence of the assumptions made for the resolution of (4.22).

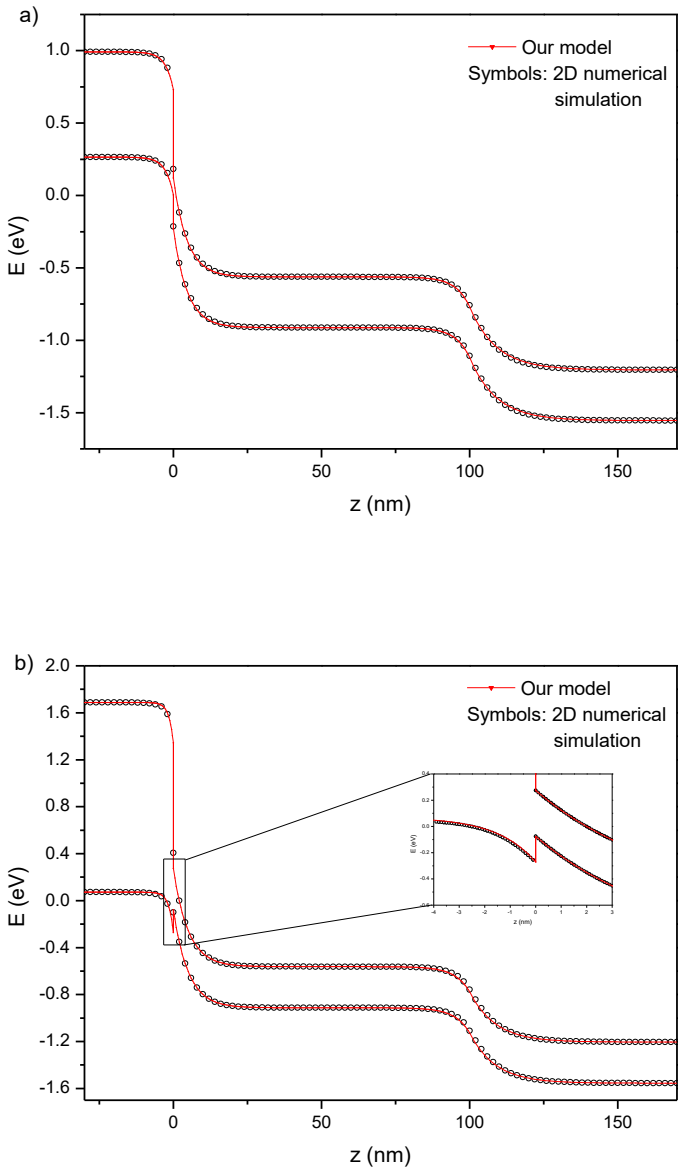

Figure 4.2 – Energy band diagram of (a) GaSb-InAs and (b) AlSb-InAs for N_{AS}=10^{20} cm^{-3}, N_{DD}=10^{19} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, L_d=70 nm, V_g=1 V, V_{ds}=0.5 V, Φ_m=5.1 eV. (notice that InAs definition in atlas is different from the cubic III-V interpolation model set [10] yielding for GaSb-InAs heterojunction staggered- or nearly broken-gap while it should be broken).

Furthermore, it is important to emphasize that the numerical results were obtained without the activation of the tunneling model. Indeed, the carriers' injection that results from the tunneling process creates charge dipoles which affect the electrostatic distribution near the tunneling junctions. A correct resolution of the problem implies the use of an iterative

scheme which is not without increasing the computation time. However, it is preferred in this study to make use of fitting parameters such as α in (4.27, 4.29) to calibrate the tunneling current.

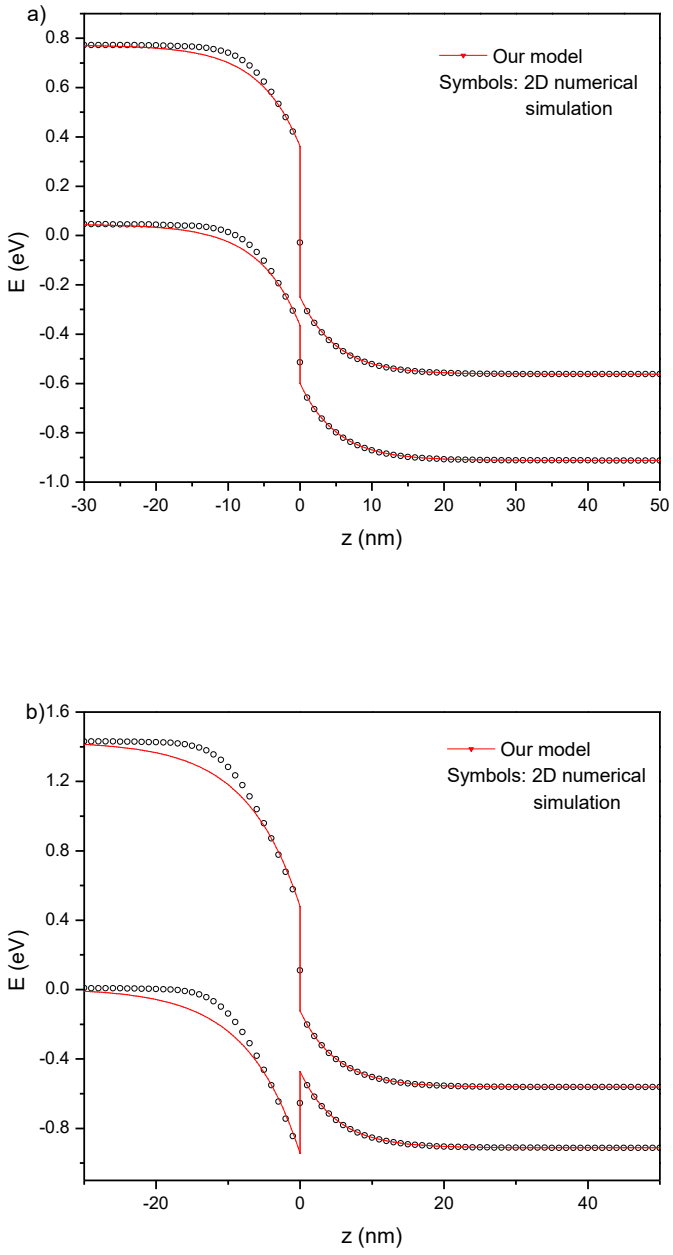

Figure 4.3 – Energy band diagram of (a) GaSb-InAs and (b) GaAs-InAs for N_{AS}=10^{19} cm^{-3}, N_{DD}=10^{19} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, V_g=1 V, V_{ds}=0.5 V, Φ_m=5.1 eV.

4.4. Tunneling current model

As aforementioned, a non-local tunneling model is presently considered in this study. Thus, the tunneling current is evaluated for all the possible electron tunneling paths comprised between the source valence band and the channel conduction band in the case of the source junction. For the drain side, the evaluation is performed between the channel valence band and the drain conduction band. Therefore, the tunneling current density takes the form [10]:

$$J = \frac{q}{\pi\hbar}\iint T(E)\left[f_l(E+E_T) - f_r(E+E_T)\right]\rho(E_T)\,dE dE_T \tag{4.33}$$

E and E_T are respectively the lateral and transverse electron energy. $\rho(E_T)$ represents the 2-D density of states that corresponds to the remaining transverse wavevectors and equals:

$$\rho(E_T) = \frac{\sqrt{m_e m_h}}{2\pi\hbar^2} \tag{4.34}$$

where m_e and m_h represent the electron and the hole effective masses that include the tunneling contribution of each conduction band valley (ex: 6 for Silicon) and both light hole and heavy hole valence band. For isotropic band structure, m_e and m_h equal respectively the electron and holes density of states masses. For binary and ternary materials, the electron effective mass is related to conduction band valley corresponding to the minimum energy bandgap [10]. As this work is more qualitative than quantitative, the density of states definition is used for all materials which is found to give a close result.

As discussed before, the Fermi occupancy difference accounts for the Landauer's conduction formula and permits to obtain a null current for zero external applied voltage. The Fermi-Dirac distribution functions for the left or right side of the tunneling junction are defined by:

$$f_{l,r}(E+E_T) = \left(1+\exp\left(\frac{E+E_T-E_{fl,r}}{KT}\right)\right)^{-1} \tag{4.35}$$

Integrating once (4.33) with respect to the transverse energy from 0 to E_{max}=min(E_l-E E-E_r), which ensures the limitation of the total carrier energy (E+E_T) to the tunneling window, we obtain:

$$I_t = \frac{qKT}{\pi\hbar}\rho\left(E_T\right)\int_0^a\int_{E_l}^{E_r} 2\pi r T\left(E\right)\log\left[\frac{\left(1+\exp\left(\frac{E_{fr}-E}{KT}\right)\right)\left(1+\exp\left(\frac{E_{fl}-E-E_{\max}}{KT}\right)\right)}{\left(1+\exp\left(\frac{E_{fl}-E}{KT}\right)\right)\left(1+\exp\left(\frac{E_{fl,r}-E-E_{\max}}{KT}\right)\right)}\right]dEdr$$

(4.36)

$$T\left(E\right)=\exp\left(-2\int_{z_1}^{z_2}\kappa(z)dz\right) \tag{4.37}$$

The tunneling probability $T(E)$ is calculated using the WKB approximation. Normally, a valid dispersion relation that links the two bands imaginary wavevector should be used as the widely Kane's two-band model [10, 19, 20]. Nevertheless, the analytical integral action of such relation is an intractable task. Therefore, the tunneling path is divided between the valence and conduction band associated wavevectors (κ_c and κ_v) with a branch point z_0 that should be carefully chosen with the aim of reproducing the original tunneling probability variation. It is worth mentioning that the branch point as used in this study doesn't carry the complete physics inside the forbidden region but is rather a practical solution that yields acceptable results. The precedent equation is then rewritten as:

$$T\left(E\right)=\exp\left(-2\left(\int_{z_1}^{z_0}\kappa_v(z)dz+\int_{z_0}^{z_2}\kappa_c(z)dz\right)\right) \tag{4.38}$$

where $\kappa_c(z)=\frac{1}{i\hbar}\sqrt{2m_0m_e(z)\left(E-E_c(z)\right)}$ and $\kappa_v(z)=\frac{1}{i\hbar}\sqrt{2m_0m_h(z)\left(E_v(z)-E\right)}$

with $m_e=\left(m_l m_t^2\right)^{1/3}$ and $m_h=\left(m_{lh}^{3/2}+m_{hh}^{3/2}\right)^{2/3}$

m_0, $m_e(z)$, $m_h(z)$, m_l, m_t, m_{lh} and m_{hh} represent respectively the electron rest mass, the position dependent electron and holes effective masses (equivalent to the density of states ones), the lateral and transverse electron masses, the light hole and heavy hole masses. Because the tunneling barrier is assumed to have an exponential profile in all the device

regions, the integral of the imaginary wavevector between the classical turning points z_1 and z_2 can be performed analytically. These latter are obtained by solving the equation $E_{c,v}$=E. Using the valence and conduction bands expressions for each region, the associated wavevectors can be written as:

$$\kappa(z)=\frac{1}{i\hbar}\sqrt{2m_0m_e(z)\left(A+B\exp(Cz)\right)} \tag{4.39}$$

Hence, the analytical integral of the wavevectors over any tunneling path gives:

$$\int_{z_1}^{z_2}\kappa(z)dz=\frac{\sqrt{2m_0m_e(z)}}{i\hbar}\left[\frac{\sqrt{A+B\exp(Cz)}-\sqrt{A}\tanh^{-1}\left(\frac{\sqrt{A+B\exp(Cz)}}{\sqrt{A}}\right)}{C}\right]_{z_1}^{z_2} \tag{4.40}$$

The heterojunction TFET energy band diagram for staggered- or nearly broken-gap (fig 4.4) shows that the tunneling window must be divided into 4 regions or energy Intervals depending on the position of the turning points.

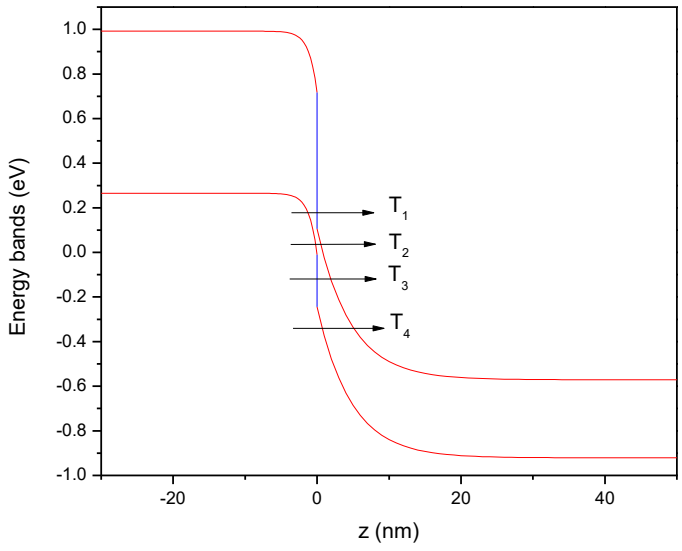

Figure 4.4 – Staggered-gap heterojunction TFET energy band diagram.

In the 1st region, the tunneling starts from the source valence band and ends at the junction conduction band. The branch point is located very close to the junction and the tunneling probability in this case is dominated by the valence band wavevector as in (4.41.a). In the 2nd region, the electrons tunnel from the source valence band to the channel conduction band. Conversely to other studies in which the branch point is set exactly at the junction interface [4, 8, 9], a branch point located into the source side was found to give better results; consequently, the probability includes three components as in (4.41.b). The 3rd region tunneling probability is dominated by the channel conduction band corresponding wavevector; therefore, the branch point is located closely to the start turning point (4.41.c). Finally, the tunneling in 4th region occurs exclusively in the channel (4.41.d). The branch point in this case is set to approximately at 20 % of the tunneling distance from the starting turning point.

For $E >= (\text{-}V_{ps}(a) \text{-} E_{is})$ & $E >= (\text{-}V_{ps}^{*}(a) \text{-} E_{ic} + E_{gc})$

$$T_1(E) = \exp\left(-2\left(\int_{z_1}^{z_0} \kappa_{vs}(z)dz + \int_{z_0}^{z_2} \kappa_{cs}(z)dz \right) \right) \text{ and } \rho_1(E_T) = \frac{\sqrt{m_{es} m_{hs}}}{2\pi\hbar^2} \quad (4.41.a)$$

For $E >= (\text{-}V_{ps}(a) \text{-} E_{is})$ & $E < (\text{-}V_{ps}^{*}(a) \text{-} E_{ic} + E_{gc})$

$$T_2(E) = \exp\left(-2\left(\int_{z_1}^{z_0} \kappa_{vs}(z)dz + \int_{z_0}^{0} \kappa_{cs}(z)dz + \int_{0}^{z_2} \kappa_{cc}(z)dz \right) \right) \text{ and } \rho_2(E_T) = \frac{\sqrt{m_{ec} m_{hs}}}{2\pi\hbar^2} \quad (4.41.b)$$

For $E < (\text{-}V_{ps}(a) \text{-} E_{is})$ & $E >= (\text{-}V_{ps}^{*}(a) \text{-} E_{ic})$

$$T_3(E) = \exp\left(-2\left(\int_{z_1}^{z_0} \kappa_{vc}(z)dz + \int_{z_0}^{z_2} \kappa_{cc}(z)dz \right) \right) \text{ and } \rho_3(E_T) = \frac{\sqrt{m_{ec} m_{hs}}}{2\pi\hbar^2} \quad (4.41.c)$$

For $E < (\text{-}V_{ps}(a) \text{-} E_{is})$ & $E < (\text{-}V_{ps}^{*}(a) \text{-} E_{ic})$

$$T_4(E) = \exp\left(-2\left(\int_{z_1}^{z_0} \kappa_{vc}(z)dz + \int_{z_0}^{z_2} \kappa_{cc}(z)dz \right) \right) \text{ and } \rho_4(E_T) = \frac{\sqrt{m_{ec} m_{hc}}}{2\pi\hbar^2} \quad (4.41.d)$$

The total tunneling probability as a function of the tunneling path energy is computed by $T(E)=\sum_i T_i(E)\left(H\left(E_i^u-E\right)-H\left(E_i^l-E\right)\right)$, where $H(E)$ is the Heaviside step function applied for each tunneling region of index i comprised between the upper and lower energies E^u and E^l. Also, as each tunneling region has its proper density of states, $\rho(E_T)$ must be reinserted under the integral sign. On the other side, the drain tunneling junction is divided into two energy intervals. The first one evaluates the tunneling probability from the channel valence band to the drain conduction band with a branch point located into this latter while the second permits to compute the tunneling probability into the drain extension. As a matter of fact, in straddled-gap heterostructure configurations, a tunneling barrier results from the valence band discontinuity at the junction (fig 4.5). This latter may attenuate further the current transport which is dominated by thermionic and field emission mechanisms [21].

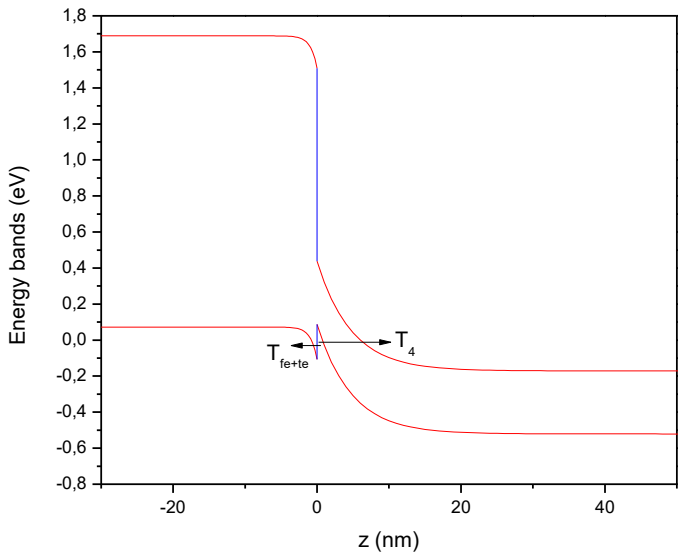

Figure 4.5 – Straddled-gap heterojunction TFET energy band diagram.

Avoiding more modeling complexity, the transport attenuation is included in an expression that reduces the tunneling probability in the 4th region by moving the branch point toward the conduction band defined as:

$$z_0 = z_1 + 0.15\left(1+\Delta E_v\right) L_t \qquad (4.42)$$

with L_t being the tunneling distance. The following figures show the good agreement of the developed model with its 2-D numerical simulation counterpart. It is noticed that the model was calibrated to cover a wide range of material configurations and parameters by means of particular branch point position and tunneling probability coefficient for each tunneling region. Also, a relative error arises from the multiple assumptions on the potential model and tunneling probability expressions. In addition, simulations show that the electron and hole quasi Fermi levels, particularly near the heterojunction interface, differ slightly from the assumed values (i.e. $-V_d$ and $-V_s$). Consequently, the tunneling current is overestimated by larger occupancy factor.

Analyzing the source doping effect, fig 4.6 shows that the doping concentration increase moves the tunneling onset to lower gate voltages. This effect is common to all materials configurations and is a consequence of the source valence band elevation. Nevertheless, a very high degeneracy, i.e. E_{vs}-E_{fs} >> 3KT, causes the tunneling onset in energy states of lower occupation factor. The current variation with respect to the gate voltage is therefore reduced and degraded subthreshold slope is obtained [6].

The case of GaSb-InAs heterojunction illustrates perfectly this effect (fig 4.6.a) where a low doping is preferable if steep subthreshold slope and high current are desired. However, this performance is limited to a certain gate voltage interval. If we consider also the ambipolar current, it is clear that low source doping can be advantageous only for small supplies.

On the other hand, a moderate doping of $5\text{x}10^{19}$ cm^{-3} offers the better compromise between the subthreshold slope and the on-current. In the case of straddled alignment as in AlSb-InAs, the behavior is totally different. Indeed, it is observed that the tunneling current is proportional to the source doping while the subthreshold slope remains unaffected either for high or moderate concentrations. This can be explained by the predominance of the tunneling in the channel (T_4) on the total current. Also, the low doping depicts the case where the valence band lies below the Fermi level yielding a narrowing of the tunneling window and a drastic degradation of the current.

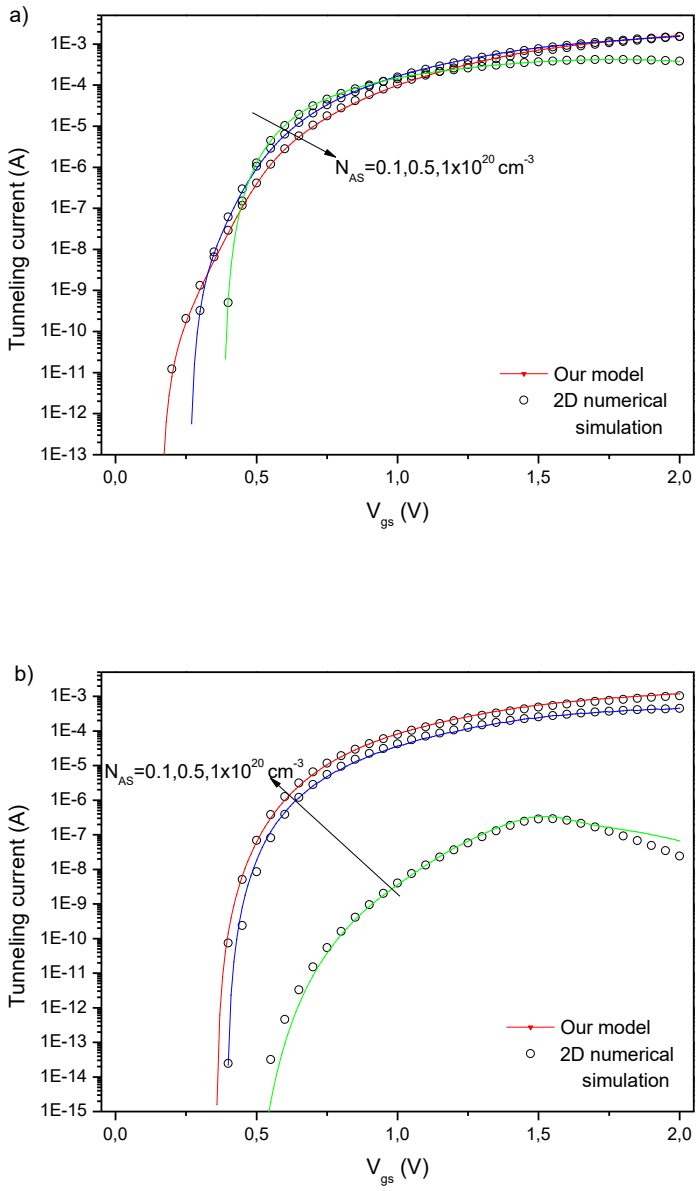

Figure 4.6 – Transfer characteristic of (a) GaSb-InAs and (b) AlSb-InAs heterojunction TFET for different source doping for t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, V_{ds}=1 V, Φ_m=5.1 eV

The effect of the device diameter is illustrated in fig 4.7. As demonstrated in the previous chapter for the local model, an improvement of the current and the subthreshold slope is observed with the diameter reduction which results from the scaling length decrease that improves the electrostatic controllability. However, this performance is limited for small

gate voltages. As the supply increases, the tunneling process is enhanced deeper in the channel. Consequently, a larger junction area will produce a higher current and thus either for straddled- or broken-gap heterojunctions.

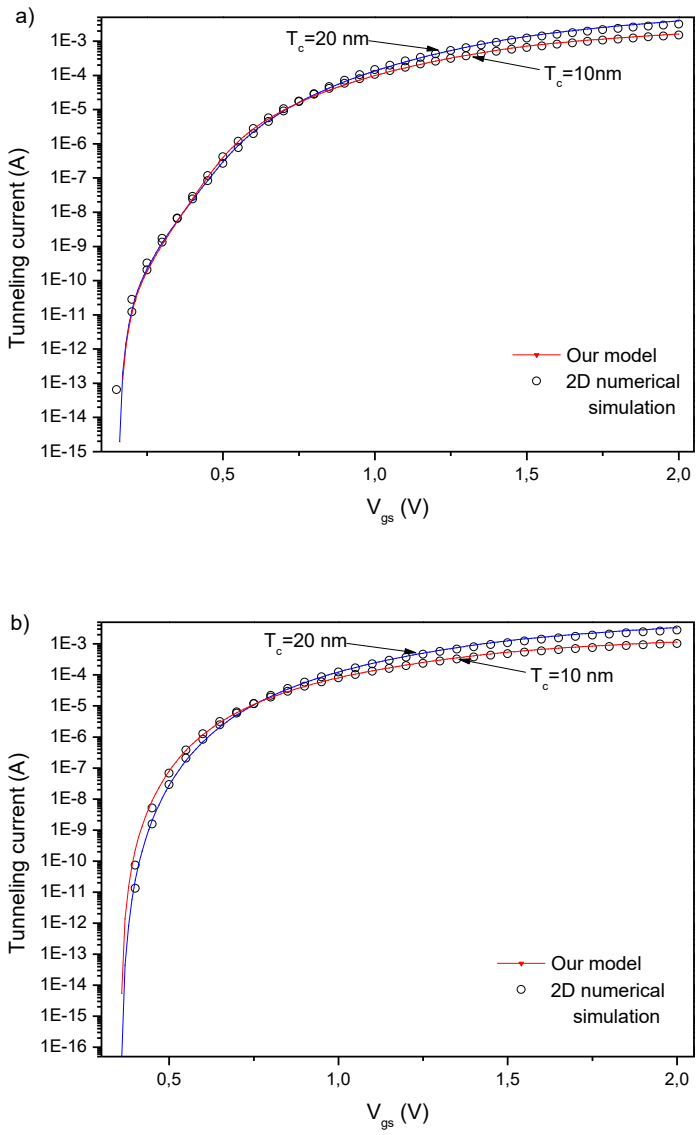

Figure 4.7 – Transfer characteristic of (a) GaSb-InAs and (b) AlSb-InAs heterojunction TFET for different diameters for N_{AS}=10^{20} cm^{-3}, t_{ox}=3 nm, L=100 nm, L_s=30 nm, V_{ds}=1 V, Φ_m=5.1 eV.

Regarding the impact of the source material definition, it is observed that the broken-gap heterostructure provides the highest current with almost 2 orders of magnitude in comparison with straddled-gap heterostructure (fig 4.8). This is a direct consequence of the tunneling probability enhancement with a peak that approaches 1 in the 1st tunneling region (fig 4.9). Nevertheless, this high tunneling probability being located in low occupation states is therefore attenuated. In such case, lower source doping shifts this peak to higher occupation states which explains the improvement observed in fig 4.6.a.

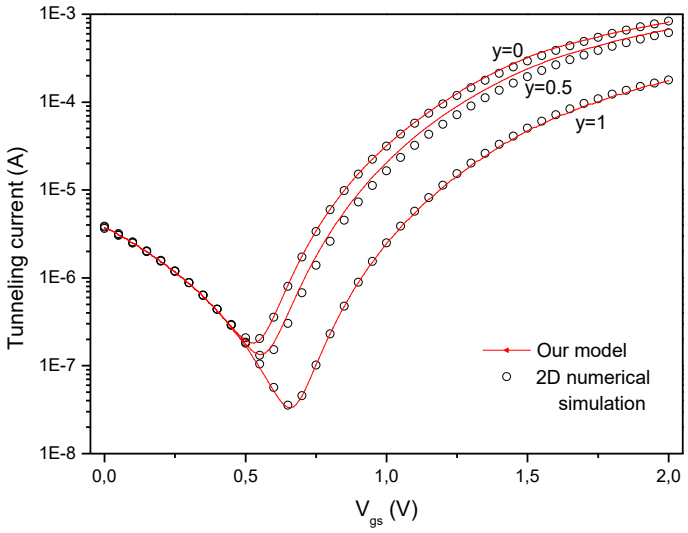

Figure 4.8 – $GaAs_ySb_{1-y}$-$In_{0.6}Ga_{0.4}As$ transfer characteristic for different As molar fraction for N_{AS}=10^{20} cm^{-3}, N_{DD}=10^{19} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, L_d=70 nm, V_{ds}=1 V, Φ_m=5.1 eV.

Moreover, the broken-gap alignment (GaSb-InAs) presents an energy region where the conduction and valence band discontinuities overlap. Named notch potential [3, 22], this region has a zero band to band tunneling probability denoted T_{no}. Nevertheless, for non-confined systems as in the present study, the combination of the high 3-D density of states in the notch potential even with a small scattering rate results in an important off-state current while the subthreshold slope easily surpasses 60 mV/dec [3]. Because the present model includes the ambipolar current, we can assume that it largely exceeds the notch

potential current even for low drain supplies (I_{off} = 58 nA @V_{ds} = 0.2 V for GaAs-InAs). Thus, the notch potential current can be neglected.

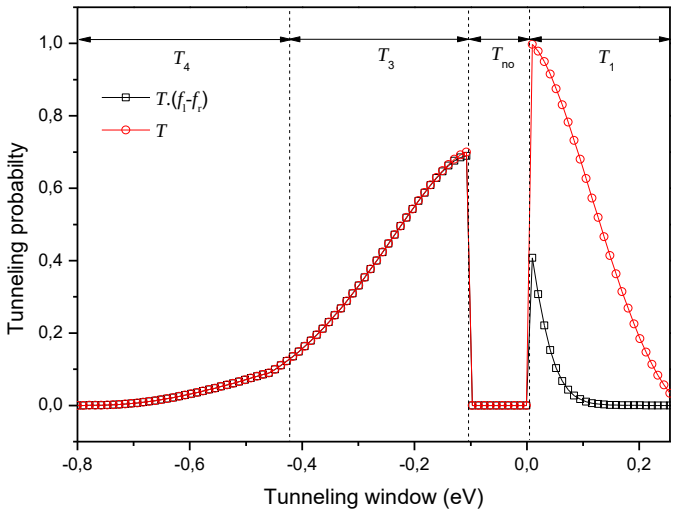

Figure 4.9 – Tunneling probability distribution over the tunneling window of broken-gap GaSb-InAs heterojunction TFETs with N_{AS}=10^{20} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, V_{gs}=1 V, V_{ds}=1 V, Φ_m=5.1 eV.

For the nearly broken- and staggered-gap alignments such as for $GaAs_{0.5}Sb_{0.5}$-InAs in fig 4.10, GaSb-$In_{0.6}Ga_{0.4}As$ and $GaAs_{0.5}Sb_{0.5}$-$In_{0.6}Ga_{0.4}As$ in fig 4.8, the four tunneling regions are operational with high tunneling probability. However, this tunneling probability and hence the current decreases with the augmentation of the As molar fraction as a consequence of the bandgap enlargement and carriers' effective masses enhancement. The tunneling current decreases further when moving toward straddled-gap configuration as a result of the tunneling probability degradation (fig 4.10). Moreover, the current composition is reduced from 4 to 2 or 3 components with the predominance of the 4th one (T_4) (depending on bands alignment, the 1st component onset occurs for high gate biases and is generally negligible). This component yields the weakest tunneling probability and is further attenuated by large valance band discontinuity that acts to reduce further the carriers drift from the source to the channel.

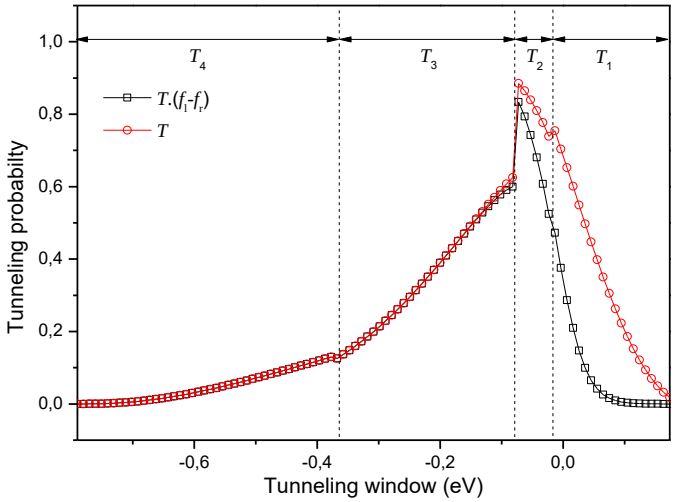

Figure 4.10 – Tunneling probability distribution over the tunneling window of staggered-gap $GaAs_{0.5}Sb_{0.5}$-InAs heterojunction TFETs with N_{AS}=10^{20} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, V_{gs}=1 V, V_{ds}=1 V, Φ_m=5.1 eV.

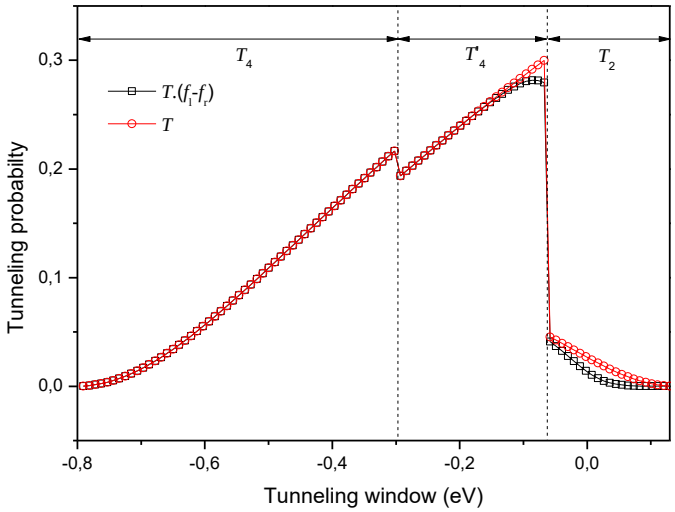

Figure 4.11 – Tunneling probability distribution over the tunneling window of straddled-gap GaAs-InAs heterojunction TFETs with N_{AS}=10^{20} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, V_{gs}=1 V, V_{ds}=1 V, Φ_m=5.1 eV.

Also, fig 4.8 shows that the off-current increases as a consequence of the source tunneling current enhancement. On the other hand, the subthreshold slope is barely affected by the band alignment as SS_{min} of 67.66 mV/dec and 66.38 mV/dec were obtained for 0 and 1 As molar fraction.

The impact of the channel and drain material definition is depicted in fig 4.12. As expected, an inverse proportionality of the total current to the material bandgap is observed. Besides the decrease of the tunneling probability (longer tunneling distance and increased effective masses), larger bandgap leads to a reduction of the heterojunction bands discontinuity and in the case of broken-gap, to the tightening of the tunneling window of the 1st and 3rd current components.

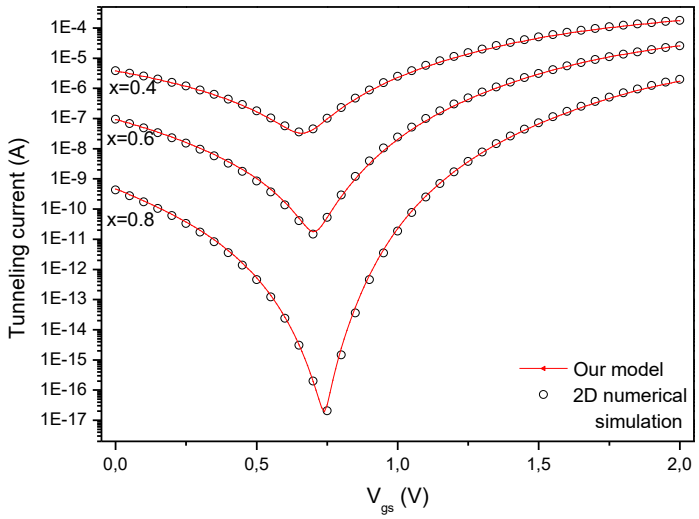

Figure 4.12 – GaAs-$In_{1-x}Ga_xAs$ transfer characteristic for different Ga molar fraction for N_{AS}=10^{20} cm^{-3}, N_{DD}=10^{19} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, L_d=70 nm, V_{ds}=1 V, Φ_m=5.1 eV.

Moreover, increasing the bandgap improves the subthreshold slope by means of the ambipolar current reduction. A SS_{min} of 18.55 mV/dec is obtained for 0.8 Ga molar fraction (E_g = 1.13 eV) while 66.44 mV/dec is found for 0.4 fraction (E_g = 0.67 eV). Furthermore, it is observed that materials with low intrinsic density of states and to a lesser extent low permittivity can prolong the gate modulation to higher voltages. Therefore, thinner

tunneling junctions can be formed with respect to the gate voltage variation which in final yields smaller average subthreshold slopes. For instance, the average subthreshold slope which is defined here as $SS_{avg}=V_{ds}/(\log_{10}(I_{on}/I_{min}))$ gives values of 293.57 mV/dec and 96.92 mV/dec for 0.4 and 0.8 Ga molar fraction respectively @ V_{ds}=1V.

Another manner of reducing the ambipolar current is to simply decrease the drain supply. By doing so, the tunneling window in the drain side is narrowed while the barrier is enlarged. Nevertheless, the gate modulation interval is also reduced which attenuates the source tunneling current for higher gate voltages. This attenuation can vary in importance with respect to the material properties. The combination of low drain voltage and narrow bandgap materials reduces the gate modulation interval to less than 1V. The current drop in such cases can exceed 50%.

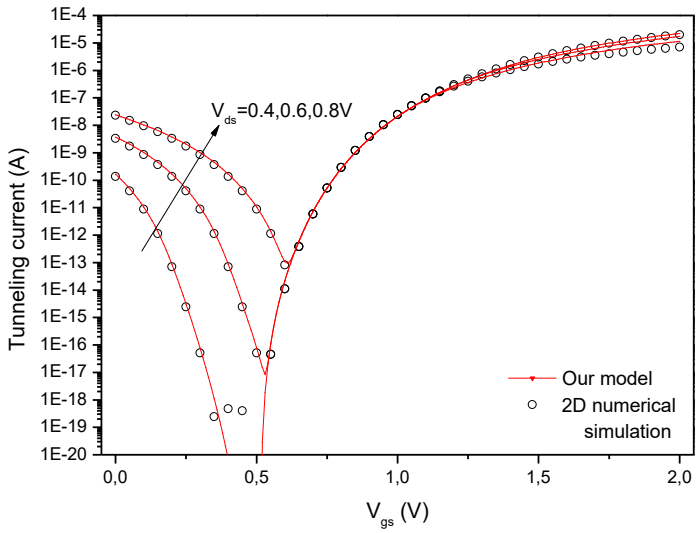

Figure 4.13 – GaAs-$In_{0.4}Ga_{0.6}As$ transfer characteristic for different drain supply for N_{AS}=10^{20}cm^{-3}, N_{DD}=10^{19} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, L_d=70 nm, Φ_m=5.1 eV.

A classical output characteristic of a TFET in the three operating region is shown in fig 4.14. According to our aforementioned clarifications, the device operation in drain modulation is equivalent to ohmic region. The heterojunction TFET current evolves either in a superlinear or sublinear slope resulting in a variable on-resistance. This slope depends essentially on the

heterostructure alignment type and source doping in the way they can provide high tunneling probability at high occupied states. It is also noticed that the disparity between the model and numerical results is a consequence of the channel potential solution which is based on the Boltzmann statistics.

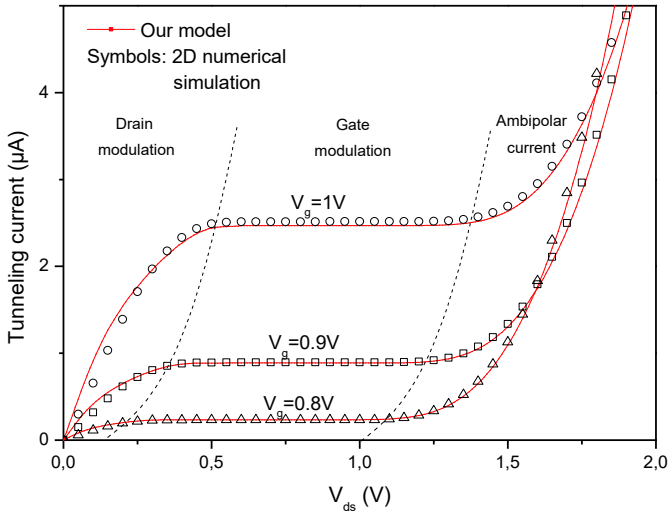

Figure 4.14 – GaAs-$In_{0.6}Ga_{0.4}As$ output characteristic for different gate voltages for N_{AS}=10^{20} cm^{-3}, N_{DD}=10^{19} cm^{-3}, t_{ox}=3 nm, T_c=10 nm, L=100 nm, L_s=30 nm, L_d=70 nm, Φ_m=5.1 eV.

Likewise, the gate modulation that corresponds to the saturation region exhibits a very low output conductance which is ideal for gain enhancement. On the other hand, the ambipolar conduction that behaves as a breakdown, limits the device supply to very low values in comparison with conventional MOSEFTs. The figure depicts also the delayed saturation that yields some issues for digital or analog application (degradation of the noise margin and gain). An attenuation of the delayed saturation and ambipolar current is possible by enlarging the channel and drain bandgaps at the expense of the saturation current.

Thus, the device material definitions can be a powerful tool to meet or even surpass the actual and future technology requirements for low power or high performance applications. However, it should be noticed that these results, especially the high on-current values, were obtained without the consideration of the mobility degradation or contact resistance

limitation. Nevertheless, most III-V compounds are characterized with high mobility. Thus, the transport limitation of the channel shouldn't be very important. Moreover, the lattice mismatch at the heterojunction interface is neglected. As explained earlier, a high defective interface yields important leakage current by means of TAT and SRH generation resulting in much higher off-state current and subthreshold slope [5, 23]. Likewise, an interfacial layer might create from abrupt heterostructure formation that alters the band alignment and degrades further the device performances, a formation of $GaAs_{0.022}Sb_{0.978}$ layer at GaSb/InAs interface was reported in [24]. Furthermore, if in theory the Anderson's rule applies well to abrupt heterojunctions (especially in depletion [25]); many studies demonstrate the oversimplification of the rule. Indeed, experimental measures of the band offset show variable and non-negligible disparities with this model. The combination of the affinity rule and transport model error can reach critical levels. The case of a heterodiode confirms the limitation of the model by showing large disagreement of the Anderson's model with the experimental results in both quantitative and qualitative aspect [21]. Therefore, the same conclusion can be transposed to the heterojunction TFET, particularly if we consider the sensitivity of the tunneling current to the electrostatic distribution and the impact of charge dipole creation on this latter. Hence, a more realistic analysis of the device should be based on experimental band alignment with an acceptable lattice mismatch.

4.5. Capacitance model

The device capacitances are essential to assess the performance in both analog and digital application. The interest is more pronounced in the case of TFETs as measurements and simulations highlighted the large contribution of C_{gd} to the total gate capacitance and the resulting enhanced Miller effect [26]. The classical MOSFET capacitance definitions are no longer applicable and proper expressions should be developed. Recalling the general capacitance definition:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \tag{4.43}$$

where Q_i and V_j are the charge and potential associated to the terminals i and j, respectively. As proposed in [27], the gate charge Q_g is composed of the channel inversion

charge Q_c and an additional charge Q_{if} induced by the inner fringing fields from the drain junction. The former component is defined by the charge at the channel interface as:

$$Q_c = 2\pi a L' C_{ox}\left(V_g^* - V_c\right) \tag{4.44}$$

with $L' = L - \frac{1}{\lambda_c}\log\left(\frac{-E_{gc}}{V_{ps}^* - V_c}\right)$

L' accounts for the active channel length, i.e. without the tunneling junction penetration in the channel. The penetration is defined as the distance where the lateral electric field drops to a characteristic electric field that equals $\lambda_c \times E_{gc}$. The inner fringing charge on the other hand can be expressed as:

$$Q_{if} = 5/2\,\pi a^2 \varepsilon_c E_{pd\square}(a) \tag{4.45}$$

The internal drain to gate capacitance C'_{gd} can now be obtained by deriving the gate charge with respect to the drain voltage. This capacitance is placed in series with the active gate oxide capacitance as:

$$C_{gd} = C'_{ox} C'_{gd} / (C'_{ox} + C'_{gd}) \tag{4.46}$$

where $C'_{ox} = 2\pi a L' C_{ox}$

As illustrated in the following figure, the proposed capacitance model offers an acceptable fit with the numerical results and thus for a large gate bias interval. As for the tunneling current during drain modulation, the error induced by the use of Boltzmann statistics to derive the channel potential expression reverberates on the inversion and inner fringing field charges. Similarly to the current, the use of the correction expression attenuates this error. Nevertheless, this model is sufficient to evaluate capacitance in our range of interest. The figure illustrates also the impact of the channel material on the capacitance. It is observed that the bandgap narrowing shifts the capacitance characteristic toward lower gate biases as a result of the premature inversion charge formation. Moreover, higher electric field arises at the drain junction interface which slightly improves the inner fringing charge capacitance. Knowing the importance of the gate to drain capacitance on both digital and analog circuits, the channel material choice is crucial for the performance improvement.

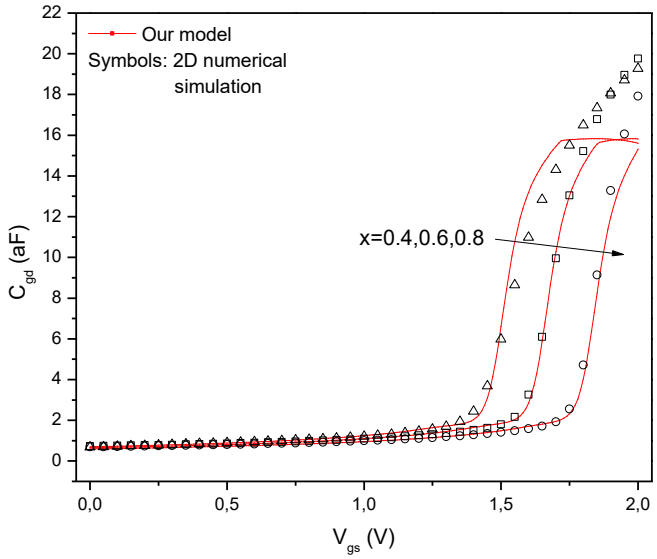

Figure 4.15 – C_{gd} for GaAs-$In_{x-1}Ga_xAs$ heterojunction TFET for different molar fraction with N_{AS}=10^{20} cm^{-3}, N_{DD}=10^{19} cm^{-3}, L=100 nm, L_d=70 nm, T_c=10 nm, t_{ox}=3 nm, V_{ds}=1 V, Φ_m=5.1 eV.

The remaining device charge corresponds to the depletion charge of the source region. Using the potential expression to evaluate the depletion width, the charge is given by:

$$Q_s = q\pi a^2 N_{AS}\left(\frac{\lambda_s^* t_{ox}}{4N_s}\right)\log\left(\frac{V_{biS}}{V_{biS}-V_{ps}}\right) \tag{4.47}$$

The derivative of this charge with respect to the source potential gives the source capacitance. Also, an additional value of approximately 1 aF that could correspond to the outer fringing capacitance was found to be necessary to match the numerical results. Nonetheless, this capacitance definition is valid only when the source tunneling junction is active as depicted in fig 4.16. In this case, the total channel charge is coupled to the drain terminal. For lower gate voltages and ambipolar state, the channel charge is transferred to the source terminal. Hence, the C_{gd} definition is transposed to the source junction. It is also observed that the channel material composition affects slightly the source capacitance by modifying the junction boundary potential and by extension, the depletion charge. The attenuation effect is more pronounced for lower Ga molar fraction, i.e. narrower bandgap,

larger valence band discontinuity and reduced gate modulation interval. Nevertheless, the C_{gs} variation during the on-state is minor with respect to C_{gd}.

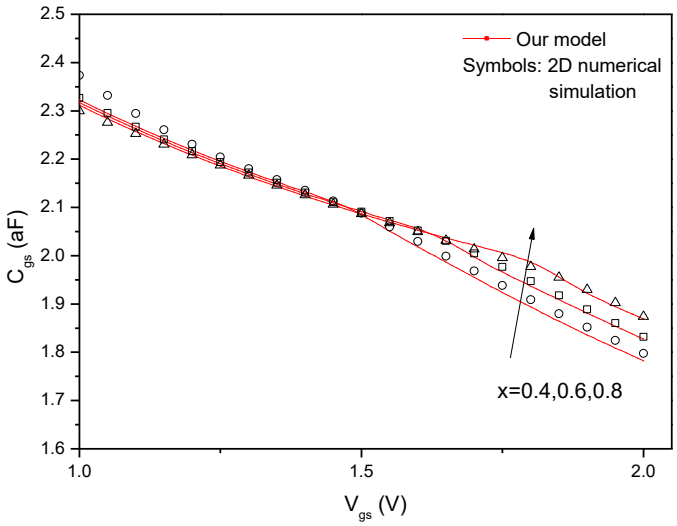

Figure 4.16 – C_{gs} for GaAs-$In_{x-1}Ga_xAs$ heterojunction TFET for different molar fraction with N_{AS}=10^{20} cm^{-3}, N_{DD}=10^{19} cm^{-3}, L=100 nm, L_s=30 nm, T_c=10 nm, t_{ox}=3 nm, V_{ds}=1 V, Φ_m=5.1 eV.

4.6. Device optimization

In this section, an optimization of the device performances in both digital and analog applications is performed. The optimization is based on a multi-objective genetic algorithm tool.

4.6.1. Digital application optimization

For the digital application, a symmetrical heterojunction TFET based inverter is considered. Also, we assume identical capacitances and equivalent resistance for the two types of device. The load capacitance C_L is defined as the sum of the internal capacitance C_{int}, which corresponds to the gate to drain capacitances of the two transistors, and the external capacitance C_{ext}. As the inverter is supposed to drive another equivalent inverter stage, C_{ext} is equivalent to the total gate capacitance. Therefore C_L can be expressed as:

$$C_L = C_{int} + C_{ext} = 2C_{gd} + 2(C_{gd} + C_{gs}) \quad (4.48)$$

The impact of the C_{gd} capacitance is clear as it is the predominant component of the load capacitance. As this capacitance is the largest component of the total gate capacitance, it controls almost all the inverter characteristics. Enhanced Miller effect is also expected in TFET based inverters which is interpreted by the overshoot/undershoot voltage amplification that generates another source of power dissipation [26]. The average on-resistance on the other hand can be approximated as [28]:

$$R_{eq} \approx \frac{3V_{DD}}{4I_{sat}} \tag{4.49}$$

The propagation delay that corresponds to the capacitance charge and discharge time is defined as $\tau_p=(\tau_{pHL}+\tau_{pLH})/2$. As the symmetry is assumed, the precedent expression can be reduced to:

$$\tau_P = 0.69 C_L R_{eq} \tag{4.50}$$

Equivalently, the rise and fall time between 10 and 90% of the output voltage with the assumption of a threshold voltage around 10% of the drain supply and a sharp transition of the input voltage can be approximated by [29]:

$$t_{r,f} = 2.2 C_L R_{eq} \tag{4.51}$$

The total power consumption over one cycle can now be evaluated as $P_{tot}=P_{dyn}+P_{sc}+P_{stat}$, where each power term represents by order the dynamic, short-circuit and static power consumptions. These powers have for definition:

$$P_{dyn} = C_L V_{DD}^2 f \tag{4.52.a}$$

$$P_{sc} = I_{peak} V_{DD} t_{r,f} f \tag{4.52.b}$$

$$P_{stat} = I_{stat} V_{DD} \tag{4.52.c}$$

where f is the clock frequency. I_{stat} refers to the static current that includes the off-state and gate leakage currents. The latter current being not modeled in this study is therefore neglected. In the aim of matching the off-current for the different configurations, it is defined as the minimum tunneling current and the corresponding gate bias V_{gsmin} as the

zero voltage reference. As large channel bandgap materials can achieve very low I_{off} and even possibly yielding a gate voltage interval where both source and drain tunneling junctions are closed, a minimum value of 1 pA/µm is applied as a reasonable limit, especially as the TAT and SRH generations are not modeled. Likewise, the transfer characteristic can be shifted to match the I_{min} with the zero gate voltage by reducing the gate work function. Accordingly, the saturation current I_{stat} is obtained for V_{gs}=V_{gsmin}+V_{DD} and V_{ds}=V_{DD} while the short-circuit peak current I_{peak} corresponds to V_{gs}=V_{gsmin}+$V_{DD}/2$ and V_{ds}= $V_{DD}/2$.

The multi objective optimization is started with a population of 200 individuals. The next generation parents are selected by tournament between two randomly chosen individuals. The reproduction is set to 80% by indeterminate crossover of the parents' genes and 20% by mutation dependent on the variables constraints. Also, 20% of the best individuals are set to migrate to the last subpopulation every 20 generations. Moreover, the Pareto front is chosen as output with a population fraction of 40%. On the other hand, the function and constraint tolerances applied to the Pareto solutions are set to 10^{-4} and 10^{-6}, respectively. The simulation framework parameters are recapitulated in the following table.

Table 4.1 – Multi objective genetic algorithm simulation parameters.

Parameters	Definitions
Source material	$GaAs_ySb_{1-y}$
Channel/drain material	$In_{1-x}Ga_xAs$
L_c (nm)	100
Ls (nm)	30
L_d (nm)	70
N_{DD} (cm^{-3})	10^{19}
N_{AS} (cm^{-3})	10^{19}-10^{20}
T_c (nm)	10-20
t_{ox} (nm)	3
t_g (nm)	1
V_{DD} (V)	0.75
Φ_m (eV)	5.1

The optimization variables are at the number of 4. The source and channel/drain materials composition for which the As and Ga molar fractions varies between 0 and 1. This ensures the performances analysis of the three possible alignment types. The source doping variation permits also to obtain the best compromise between the on- and off-state currents. Similarly, the channel diameter plays an important role on the device performances, particularly the saturation current and capacitances. Furthermore, the propagation delay and total power consumption are chosen as outputs as these parameters represent the key features of the inverter and more generally digital applications performances. The optimization results are presented in the next figure.

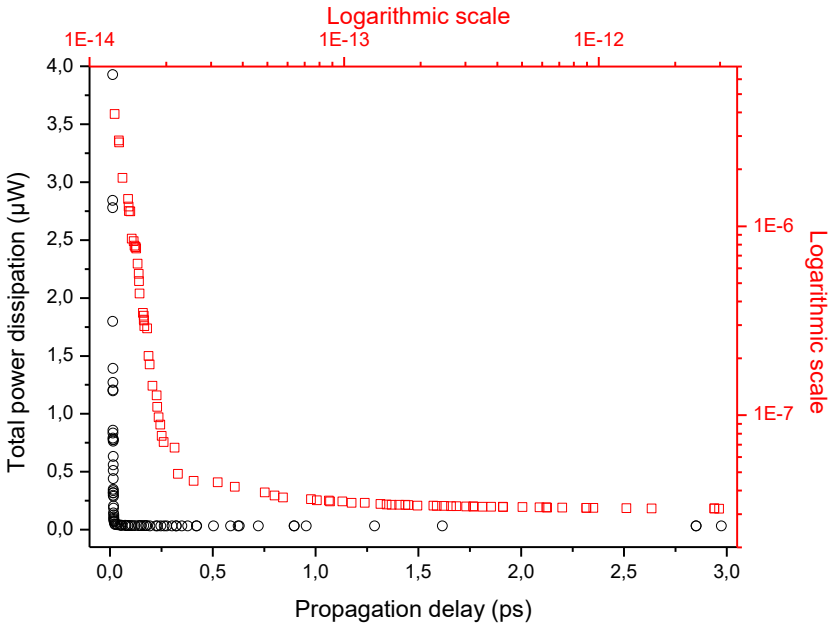

Figure 4.17 – Pareto front obtained using multi objective optimization for the heterojunction TFET based inverter, linear and logarithmic scales.

The Pareto solution shows a minimum power consumption of 32 nW that was obtained for 0.9838 Ga and 0.0296 As molar fractions, 10 nm of channel diameter and a moderate doping of 6.1×10^{19} cm^{-3}. This parameters set corresponds to a staggered-gap heterostructure with large valence band discontinuity and a E_{gs} of a 0.706 eV, smaller than the $E_{gc,d}$ of 1.397 eV.. This structure exhibits also a low I_{off} of 41.19 fA and an SS_{avg} of

99.29 mV/dec. Accordingly, a very low P_{stat} of 30.89 fW is obtained. The propagation delay on the other hand reaches the highest value of 2.97 ps.

On the opposite side, with a load capacitance of 35.77 aF, a minimum propagation delay of 12.55 fs was obtained for 0.1903 Ga and 0.08 As molar fractions, 15.42 nm of channel diameter and a low doping of 1.513×10^{19} cm^{-3}. This parameters set corresponds to a nearly broken-gap heterostructure with a E_{gs} of 0.677 eV and a $E_{gc,d}$ of 0.484 eV. This configuration yields also a high leakage current of 5.05 µA which results in static power dissipation greater than the active power (3.79 µW and 0.1 µW respectively). The SS_{avg} on the other hand degrades to 320.48 mV/dec.

The best compromise between the two output parameters 31.88 fs and 44.19 nW is obtained for 0.3962 Ga and 0.0314 As molar fractions, 10.80 nm of channel diameter and a low doping of 2.482×10^{19} cm^{-3}. Such parameters set corresponds to a staggered-gap heterostructure with a E_{gs} of 0.705 eV and $E_{gc,d}$ of 0.663 eV. Notice that the bands discontinuity proportion ΔE_c:ΔE_v is about 52:48 %. The device achieves also a I_{sat}/I_{off} ratio of 2×10^4 and an SS_{avg} of 174.09 mV/dec. The P_{dyn} is more than 4 times greater than P_{stat} and almost 5 times than P_{sc}.

Overall, the carried out optimization permits to propose design rules for heterojunction TFET based inverters and logic circuits. As illustrated in fig 4.18, if high performance is desired, nearly broken-gap heterojunction with low source doping and medium channel diameter should be used. If low power is targeted, staggered-gap heterojunction with the source as the narrower bandgap material with a moderate doping and small channel diameter should be employed. Likewise, if a compromise between the two performances is preferred, the device configuration should be based on staggered-gap heterojunction with approximately equivalent source/channel bandgaps and conduction/valence band discontinuities (bands discontinuity proportion ΔE_c:ΔE_v not exceeding 53:47 %) , a relatively low source doping (between 2.4×10^{19} and 5×10^{19} cm^{-3}) and a small channel diameter.

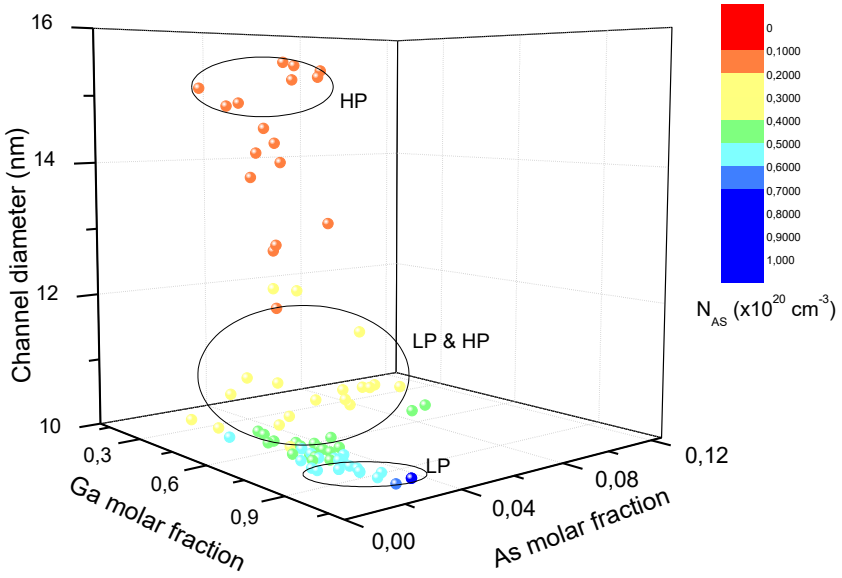

Figure 4.18 – A 3-D visualization of input configurations associated to the optimized heterojunction TFET based inverter.

4.6.2. Analog/RF application optimization

In analog/RF applications, the gain, linearity, dynamic range and bandwidth are among the most important conception key features. In this aim, a multi objective genetic framework of the intrinsic gain, 3rd order intermodulation intercept point and cutoff frequency, as defined in the previous chapter, is carried out. The simulation context and parameters are identical to the precedent computation.

As showcased by fig 4.19, the maximum intrinsic gain of 91.01 dB is obtained for 0.737 Ga and 0.03 As molar fractions, 11.22 nm of channel diameter and a high doping of 9.26×10^{19} cm^{-3}. This configuration set corresponds to a staggered-gap heterojunction with a larger valence band discontinuity, a E_{gs} of 0.706 eV and a $E_{gc,d}$ of 1.05 eV. Such configuration operating in gate modulation yields low g_m and much lower g_d. Besides, the device achieves a minimum IIP_3 of 6.73 dBm and f_t of 1.77 THz.

The maximum third order intercept power point of 71.856 dBm is obtained for 0.01 Ga and 0.4 As molar fractions, 16.78 nm of channel diameter and a high doping of 8.214×10^{19} cm^{-3}.

This configuration corresponds to a nearly broken heterojunction with a E_{gs} of 0.662 eV and a $E_{gc,d}$ of 0.36 eV. Despite of the high g_m yielded from the narrow channel bandgap, this configuration achieves a low A_v of 6 dB and a f_t of 13.71 THz consequently to the enhanced g_d and C_{gg} as the device operates in drain modulation (ohmic region).

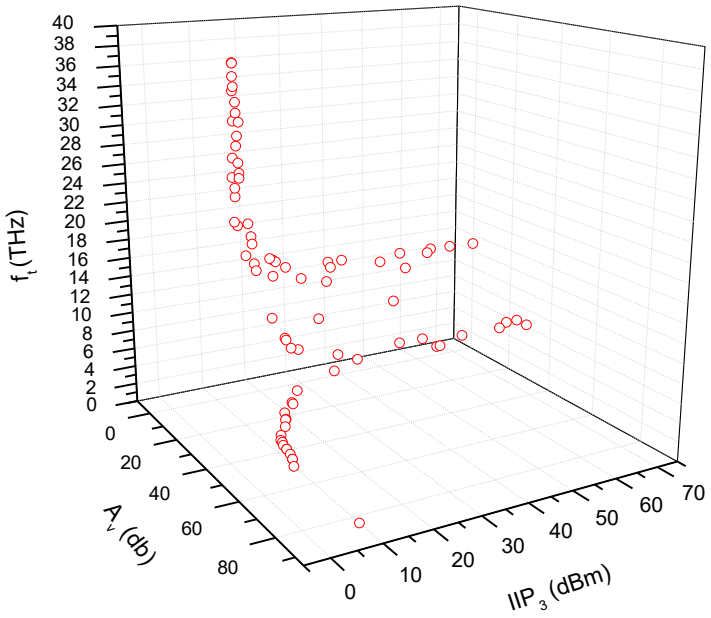

Figure 4.19 – A 3-D representation of Pareto front obtained using multi objective optimization for the heterojunction TFET based analog/RF application.

The Pareto solutions show also a second configuration that yields high IIP_3 of 71.41 dBm for 0.607 Ga and 0.122 As molar fractions, 11.37 nm of channel diameter and a moderate source doping of 6.623×10^{19} cm^{-3}. This configuration set corresponds to a staggered-gap heterojunction with a E_{gs} of 0.658 eV and a $E_{gc,d}$ of 0.888 eV. The device in such case operates in gate modulation (saturation) and results in an improvement of the A_v of 34.91 dB. However, the lower g_m leads to a slightly degraded f_t of 7.3 THz.

The maximum unity gain cutoff frequency of 36.95 THz is obtained for 0.281 Ga and 0.05 As molar fractions, a medium channel diameter 14.37 nm and a low source doping of 2.15×10^{19} cm^{-3}. This configuration corresponds to a nearly broken heterojunction with a E_{gs} of 0.693 eV and a $E_{gc,d}$ of 0.558 eV. Likewise, the device that operates in drain modulation

achieves low A_v of 14.44 dB and IIP_3 of 11.03 dBm as a consequence of the enhanced g_d and g_{m3}.

The best compromise between the three output parameters with values around 30.39 dB of A_v, 18.29 dBm of IIP_3 and 8.78 THz of f_t is obtained for 0.514 Ga and 0.034 As molar fractions, 11.44 nm of channel diameter and a source doping of 8.755×10^{19} cm^{-3}. This parameters set corresponds to a staggered-gap heterostructure with a E_{gs} of 0.703 eV and $E_{gc,d}$ of 0.784 eV.

As for digital application, the achieved optimization allows to rough out a design rule for analog/RF applications. As elucidated in fig 4.20, if high intrinsic gain is targeted at the expense of linearity and bandwidth, staggered-gap heterostructure with larger channel/drain bandgap and valence band discontinuity, small channel diameter and high source doping should be used.

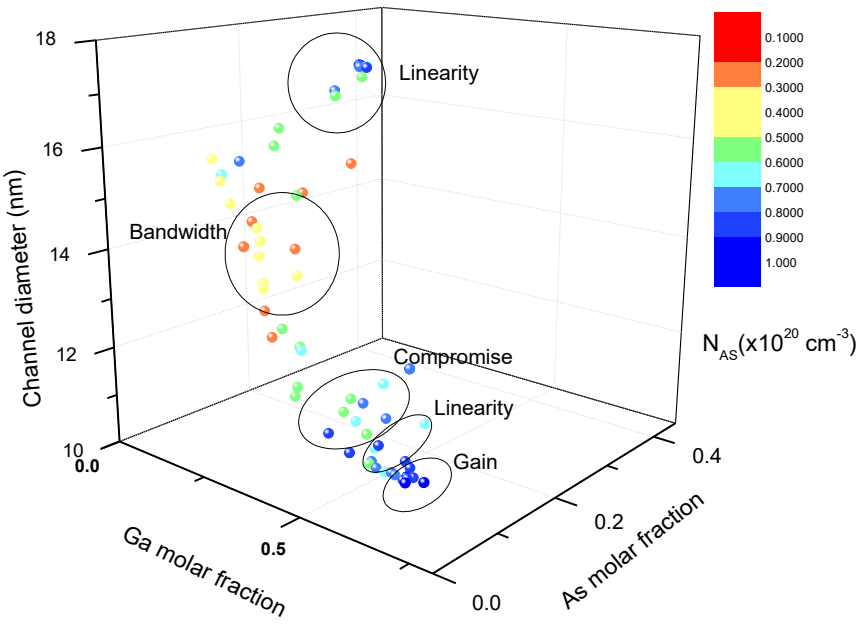

Figure 4.20 – A 3-D visualization of input configurations associated to the optimized heterojunction TFET based analog/RF application.

Likewise, if enhanced linearity and dynamic range is preferred, nearly broken heterojunction with high source doping and medium channel diameter should be employed. By decreasing the source doping to low concentrations, the latter configuration can be tuned to enhance

the cutoff frequency if a large bandwidth is desired. On the other hand, if a compromise between these characteristics is required, the configuration should be based on staggered-gap heterojunction with the source as the narrower bandgap material and bands discontinuity comprised between 40 and 60 %, moderate to high source doping and relatively small channel diameter.

4.7. Conclusion

In this chapter, a new semi-analytical model of an undoped heterojunction VSG-TFET was developed. Basing on the previous elaborated model, an appropriate exponential approximation of the channel 2-D potential valid for long channels was adopted. Expressions of the junctions' potential were derived based on both Fermi-Dirac and Boltzmann statistics to take into account the extensions degeneracy. Using conformal representation technique, suitable expressions of the source and drain extensions surface potential supporting the fringing field were developed. The heterostructure band alignment was computed using the affinity rule. The exponential potential profile over the whole device allowed the analytical integration of the tunneling probability basing on the WKB approximation. By adopting a nonlocal approach, reasonable estimation of the tunneling current was obtained by an appropriate set of the wavevectors and tunneling regions contribution. The model was validated and calibrated with 2-D numerical simulations. The demonstrated validity of the model for a wide range of device material definitions, dimensions and supplies permitted to gain insight on the heterojunction TFET physics. The model limits and lacks were highlighted as well. The impact of the possible band alignment types and source doping on the tunneling transport and device performances was argued. Analytical terminals capacitance model was also derived. The discussion showcases the tremendous possibilities provided by materials compositions and doping that permits the enhancement of a particular device feature or an ensemble of performances. The exploration of design possibilities is carried out using a multi objective genetic framework optimization. It permitted to outline new design rules for digital and analog/RF applications depending on the targeted performance. The study demonstrated the heterojunction TFET ability to match and even surpass the actual and projected technology requirements, limited only by the fabrication process constraints.

References

[1] S. Mookerjea, *et al.*, "Experimental demonstration of 100nm channel length $In_{0.53}Ga_{0.47}As$-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications," in 2009 IEEE International Electron Devices Meeting (IEDM), pp. 1–3, IEEE, dec 2009.

[2] G. Dewey, et al, "Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing," IEEE International Electron Devices Meeting (IEDM), pp. 785-788, Washington, DC, USA, 5-7 Dec. 2011.

[3] J. Knoch, J. Appenzeller, "Modeling of High-Performance p-Type III–V Heterojunction Tunnel FETs," IEEE Electron Device Letters, vol. 31, pp. 305- 307, Apr. 2010.

[4] A. S. Verhulst, W. G. Vandenberghe, K. Maex, G. Groeseneken, "Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization," Journal of Applied Physics, vol. 104, pp. 064514, Jul. 2008.

[5] C. Convertino, C. B. Zota, H Schmid, A. M. Ionescu, K. E. Moselund, "III–V heterostructure tunnel field-effect transistor," Journal of Physics: Condensed Matter, vol. 30, Jun. 2018.

[6] L. De Michielis, et al., "Tunneling and Occupancy Probabilities: How Do They Affect Tunnel-FET Behavior?," IEEE Electron Device Letters, vol. 34, pp. 726-728, Jun. 2013.

[7] Penn State III-V Tunnel FET Model Manual, https://nanohub.org/.

[8] Y. Taur, J. Wu, J. Min, "An Analytic Model for Heterojunction Tunnel FETs with Exponential Barrier," IEEE Transactions on Electron Devices, vol. 62, pp. 1399-1404, May. 2015.

[9] J. Min, J. Wu, Y. Taur, "Analysis of Source Doping Effect in Tunnel FETs With Staggered Bandgap," IEEE Electron Device Letters, vol. 36, pp. 1094-1096, Oct. 2015.

[10] ATLAS User Manual: Device Simulation Software, 2012.

[11] M. G. Bardon, H. P. Neves, R. Puers, C. V. Hoof, "Pseudo-Two-Dimensional Model for Double-Gate Tunnel FETs Considering the Junctions Depletion Regions," IEEE Transactions on Electron Devices, vol. 57, pp. 827-834, Apr. 2010.

[12] R. Vishnoi, M. J. Kumar, “A Pseudo-2-D-Analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET,” IEEE Transactions on Electron Devices, vol. 61, pp. 2264-2270, Jul. 2014.

[13] C. Shen, et al., “A Variational Approach to the Two-Dimensional Nonlinear Poisson’s Equation for the Modeling of Tunneling Transistors,” IEEE Transactions on Electron Devices, vol. 29, pp. 1252-1255, Nov. 2008.

[14] F. Jazaeri, “Modeling Junctionless Metal-Oxide-Semiconductor Field-Effect Transistor,” PhD dissertation, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, 2015.

[15] S.C. Lin, J.B. Kuo, “Modeling the fringing electric field effect on the threshold voltage of FD SOI nMOS devices with the LDD/sidewall oxide spacer structure,” IEEE Transactions on Electron Devices, vol. 50 , pp. 2559-2564, Dec. 2003.

[16] A. Bansal, B. C. Paul, K. Roy, “An Analytical Fringe Capacitance Model for Interconnects Using Conformal Mapping,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, pp. 2765-2774, Dec. 2006.

[17] R. Plonsey, R. E. Collin, “Principles and Applications of Electromagnetic Fields,” McGraw-Hill Book Company, 1961.

[18] R. L. Anderson, “Experiments On Ge-GaAs Heterojuntion,” Solid-State Electronics, vol. 5, pp. 341-344, Sep–Oct. 1962.

[19] E. O. Kane, “Zener tunneling in semiconductors,” Journal of Physics and Chemistry of Solids, vol. 12, pp. 181-188, Jan. 1960.

[20] S. Tanaka, “A unified theory of direct and indirect interband tunneling under a nonuniform electric field,” Solid-State Electronics, vol. 37, pp. 1543-1552, Aug. 1994.

[21] A. G. Milnes and D. L. Feuct, “Heterojunctions and Metal Semiconductor Junctions,” Academic Press, New York, 1972.

[22] S. O. Koswatta, S. J. Koester, W. Haensch, “On the Possibility of Obtaining MOSFET-Like Performance and Sub-60-mV/dec Swing in 1-D Broken-Gap Tunnel Transistors,” IEEE Transactions on Electron Devices, vol. 57, pp. 3222-3230, Dec. 2010.

[23] A. C. Seabaugh, Q. Zhang, “Low-Voltage Tunnel Transistors for Beyond CMOS Logic,” Proceedings of the IEEE, vol. 98, pp. 2095-2110, Dec. 2010.

[24] B. Rajamohanan, “Fabrication, Characterization and Physics of III-V Tunneling Field Effect Transistors for Low Power Logic and RF Applications,” PhD dissertation, Pennsylvania State University, 2010.

[25] M. S. Lundstrom, R.J.Schuelke, “Modeling semiconductor heterojunctions in equilibrium,” Solid-State Electronics, vol. 25, pp. 683-691, Aug. 1982.

[26] S. Mookerjea, R. Krishnan, S. Datta, V. Narayanan, “On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors,” IEEE Electron Device Letters, vol. 30, pp. 1102-1104, Oct. 2009.

[27] L. Zhang, X. Lin, J. He, M. Chan, “An Analytical Charge Model for Double-Gate Tunnel FETs,” IEEE Transactions on Electron Devices, vol. 59, pp. 3217-3223, Dec. 2012.

[28] J. M. Rabaey, A. P. Chandrakasan, B. Nikolić, “Digital integrated circuits: a design perspective,” Pearson Education, 2003.

[29] J. E. Ayers, “Digital Integrated Circuits: Analysis and Design, Second Edition,” CRC Press, 2009.

CHAPTER 5:

Investigating the HCD on JL VSG-FET

5.1. Introduction

MOSFET device reliability became a major concern for electronics industry over the past decades. The aging phenomenon was found to degrade seriously the device operation and lifetime. Extensive researches have been carried out in order to identify the causes of this process and prevent it. Channel and substrate hot carrier injection (HCI and SCI), channel hot electron/hole (CHE/H), drain avalanche injection and radiation were identified as the source mechanisms of degradation [1-7].

Hot carrier induced degradation is of prime interest for designers as an aggravation of this process is observed with the downscaling. The degradation is essentially due to the enhancement of the electric field with dimensions reduction giving, in the lucky electron model representation, the carriers enough energy to inject through the oxide layer with a probability to be captured by existing oxide traps or to break silicon bounds and hence creating new interface traps [3]. The relatively recent energy driven paradigm proposed by Rauch *et al* suggests that electron-electron scattering mechanism, governed by the energy rather than the electric field, is responsible for the HCD aggravation in downscaled devices [8]. The HCD of devices' properties is well known and the metrics degradation monitoring such as the on-current and transconductance permits an evaluation of the device lifetime [1]. At circuit level however, the assessment of the aging process is more complex and implies the use of compact models or predefined power-law degradation models [9]. These models do not take into account of the interface states profile over the gate length or their energetic distribution. To date, only the interface traps capacitance is included in advanced compact models [10]. Therefore, new models are required in order to capture the whole physics and allow reasonable estimation of circuits' degradation. In this field, some works have proposed the introduction of the interface traps charge in the surface potential expression [11]. Nevertheless, the time dependence of the traps distribution is not included.

In this optic, it would be interesting to explore the possibilities of developing new models that include the interface traps distribution in the JLFET. Especially as experimental results of stress-induced degradation demonstrate high immunity against HCD and longer lifetime of this device in comparison with its IM counterpart [12-14]. It is essential in a first step to elucidate the interface states creation and the proved reliability of the JLFET, particularly as high impact ionization rate is reached in this device, which normally would increase the

degradation. Therefore, we propose in what follows an in-depth analysis of the HCD in both JL and IM VSG-MOSFETs.

5.2. The junctionless transistor

The junctionless transistor concept was proposed by Lee *et al* [15] as a simple way to overcome the present process technique limitations. Indeed, as the downscaling trends toward channel lengths less than 10 nm, the control of the process induced variability becomes imperative to conserve the transistor properties. At such scales, the inherent scattering and diffusion of the shallow extensions impurities into the ultra-short channel poses a serious problem. Knowing that high doping concentration gradient is primordial, the extensions formation with the actual process techniques implies additional complex and costly operations (additional millisecond annealing techniques) [16]. The first study suggested that the suppression of the junctions by setting a uniform one type doping over the whole device yields a better resilience to SCEs compared to conventional MOSFET and an excellent turn-off. Soon after, Collinge *et al* successfully fabricated the first junctionless transistor with full CMOS functionality, which was named then gated resistor. The transistor was characterized with a subthreshold slope near to 60 mV/dec and a very low leakage current [16].

Because of the absence of junctions to prevent the carrier flow, the JL is considered as normally closed device (on). However, the workfunction difference between the gate and the heavily doped channel forces the carriers' depletion and hence prevents the creation of a conduction path assuring an efficient off-state. In the subthreshold regime, the JLFET operates as an accumulation mode device in depletion and small current flows by diffusion. As the gate bias is increased, a conduction channel takes place into the center of the body and keeps enlarging until it occupies the entire channel volume. At this point, the flatband condition is reached and the carriers are slightly uniformly distributed over the depth direction. The channel is then said to be electrically neutral and the transverse electric field tends toward zero. Higher gate voltage leads to the formation of an accumulation layer beneath the gate oxide. The saturation mechanism on the other hand is very similar to an IM device. As the drain bias is increased, the partial depletion near the drain increases until

a pinch-off of the conduction channel is formed. The difference is that the pinch-off is located at the body center of the JL and is caused by the electrostatic control. While in the IM devices, the pinch-off is situated beneath the gate and results from the extension of the p-n^+ junction's space charge region.

Overall, with a well sized JLFET, MOSFET like transfer and output characteristic can be obtained. The trigate gated resistor fabricated by Colinge *et al* achieved an I_{on}/I_{off} ratio of more than 10^6 and a SS of 64 mV/dec [16]. In comparison with a 20 nm trigate nMOSFET that was characterized with a SS of 92 mV/dec and a DIBL of 78 mV/V, equivalent JLFET performed a SS of 75 mV/dec and a DIBL of 10 mV/V [17]. Otherwise, the same I_{on} and I_{on}/I_{off} ratio were reported for the both devices. Furthermore, an enhanced saturation current of the JLFET in comparison with its IM counterpart is measured for the same "V_{gs}-V_{th}" voltage [17]. Conversely, Rios *et al* obtained different results from their comparative study based on matched off-state current [18]. In fact, major degradation of all the metrics of the JLFET was reported. This degradation worsens with the doping increase. Moreover, the JLFET achieves relatively lower transconductance and cut-off frequency compared to conventional MOSFET. The latter degrades further above threshold voltage with the enhancement of the total gate capacitance.

Additional transport mechanisms have been reported in JLFETs. The band to band tunneling from the channel to the drain has been identified as a source of leakage current enhancement with consequent deterioration of the subthreshold swing and DIBL, especially in narrow bandgap materials [19-21]. The impact ionization was also identified in junctionless devices [22, 23]. Experimental results demonstrate a lower II threshold energy (less than the conventional 1.5 times E_g [24]) and higher multiplication factor in comparison with the IM device. This fact is explained by the enhanced impact generation rate and electron temperature distributed over a larger volume as a result of the particular electrostatic profile. The II enhancement in the JL device can also be attributed to the bandgap narrowing induced by the high body doping [22, 23].

In addition, the two mechanisms lead to the creation of minority carriers. The accumulation of the generated holes in the channel results in a floating body effect and parasitic bipolar junction transistor (BJT). The combination of the avalanche effect due to the high II multiplication factor and the enhancement of the BJT base formed by the excess generated

holes creates a positive feedback loop mechanism. The triggering of this feedback loop is traduced by an instant current raise depicted by the kink effect in the output characteristic and a sharp subthreshold slope in the transfer characteristic [23]. Experimental results show that both IM and JL Multi-gate FET can reach a minimum SS of 5 mV/dec. However, only 2.5 V of drain supply is needed for the JLFET while 5 V is necessary for the IM device to achieve the same subthreshold slope [22]. Moreover, the generation rate enhancement in narrow bandgap materials while maintaining roughly similar recombination rate yields an impressive sharp subthreshold slope <1 mV/dec and larger magnitude of current change [25]. Additionally, a memory effect that holds the BJT feedback loop mechanism is observed as the gate voltage is swept backward. This effect is depicted by a hysteresis in the transfer characteristic, which yields two threshold voltages corresponding to the forward and backward sweep. Therefore, the dynamic operation of logic circuits (gates or memories) is altered by affecting the drive current, noise margins and propagation delay. It can also lead to undesirable and instable effects such as racing or bit reversal [26]. Nevertheless, the idea of exploiting the hysteresis characteristic as a single transistor dynamic memory is interesting, all the more so large hysteresis window can be obtained at lower drain biases and even larger with narrow bandgap materials [27]. In addition, it is important to notice that in the presence of the majority carriers of the channel, the minority carrier's recombination occurs in a continuous manner which attenuates the positive feedback loop. Consequently, a lower amount of current change, delayed kink effect and higher breakdown voltage is achieved [22, 28].

As aforementioned, the JLFET has a better immunity against SCEs. Overall, experiments and simulations demonstrate the scaling capability of the JLFET with much lower subthreshold slope (often approaching the 60 mV/dec) degradation and threshold voltage roll-off than equivalent IM transistors. The JLFET exhibits also lower DIBL which is primordial for low voltage CMOS applications [17, 28, 29]. This feature is explained by the fact that in the absence of junctions and dopant scattering, the channel effective length is sensibly equal to the gate physical length. Furthermore, the depletion at the body periphery is larger compared to its center yielding an effective length larger than the physical one which can be advantageous to reduce the SCEs [30]. The downscaling in JLFET isn't just a technological requirement but also a functionality condition. Indeed, the JLFET must have an enough thin

body and oxide layer to permit a deep and efficient electrostatic control over the entire volume ensuring the total carrier's depletion of the channel during the off-state [16]. Multigates structures are also suitable for JLFETs due their enhanced electrostatic controllability, GAA and nanowires are found to be the most efficient structures that provides full carrier's depletion for thin bodies [17, 28, 31, 32, 33]. Moreover, studies and experiments demonstrate that even at atomic scales, the JLFET still has a total functionality with good characteristics [28, 31, 33]. Furthermore, the reduction of the body thickness yields significant reduction of the threshold voltage sensitivity toward device dimensions variability. As reported by Colinge *et al*, the JLFET offers large flexibility on the threshold voltage by varying the body thickness and width while keeping the same doping and EOT [34]. If this feature represents a design advantage, it reflects also a high sensitivity to process parameter variability as the line edge roughness (LER). For instance, a device with p^+ polysilicon gate, $2x10^{19}$ cm^{-3} channel doping, 1 nm EOT and 15 nm body thickness exhibits high threshold voltage variability of 100 mV/nm. Likewise, it was demonstrated that the metrics variation induced by the Random dopant fluctuation (RDF) is comparable to the LER and is roughly similar to IM devices [34, 35]. Interestingly, it was found that the reduction of the channel thickness attenuates the RDF induced variability. Even if the volume is shrunk (which normally should worsen the variability, the impact of length reduction is more relevant [36]), it is argued that the resulting enhanced controllability is responsible for this variability attenuation [35]. Moreover, the enhancement of the ionized impurities screening might reduce further the variability.

As previously explained, one of the most interesting characteristic of the junctionless transistor is its very low transverse electric field which tends toward negligible levels when the transistor is in flatband condition [37]. Consequently, the channel carrier's mobility, especially at the surface, is supposed to be totally free from the effect of the transverse electric field. Even below the flatband condition, the conduction path is essentially located in the center of the body where the transverse electric field is much lower compared to the peripheral, yielding lesser sensitivity of the bulk carrier's mobility against the gate voltage. It is worth mentioning that the impact of the electric field on the mobility degradation is as much as important as that induced by the doping concentration increase. Nevertheless, it

was reported that the degradation attains stationary levels beyond 10^{19} cm^{-3} of doping concentration either for p- or n-type [38].

Conversely to IM MOSFETs, measures highlighted an enhancement of the effective mobility with respect to the gate bias increase [18]. The enhancement is so significant that the effective mobility exceeds the corresponding bulk mobility especially during accumulation regime [39]. A substantial improvement of the surface mobility was also observed in the accumulation layer of heavily doped devices [40], which predicts higher current during accumulation regime of the JLFET. This effect is attributed to the impact of the accumulation layer on the screening of ionized impurities, yielding a reduction of the Coulomb scattering [30, 40]. In heavily doped devices, measurements highlight the correlation between the carrier's density and the Coulomb scattering limitation where a significant improvement of the effective mobility respectively to the carrier's density is observed (largely exceeding the bulk mobility) [41, 40]. In addition, it was demonstrated that the better electrostatic controllability provided by multigates and thinner EOT yields higher carrier's density and improved mobility [41]. The improvement is more significant in thin channels as a consequence of a better screening of the reduced dopant atoms number in shallow volumes [41]. Similarly, the additional subbands filling due to quantum confinement effect in ultra-thin structures results in the increase of the carrier's density [28]. Persson *et al* proposed a more insightful explanation of the mobility enhancement [42]. They suggested that the majority carriers see the impurities as quantum wells while the transmission occurs above these latter. Therefore, increasing the screening will have no subsequent effect. Conversely, the minority carriers in IM device see the charged impurities as tunnel barriers that can strongly impede their flow. In this case, the screening effect of the gate, the gate oxide and the inversion layer reduces effectively the impurity potential barrier. Persson *et al* concluded that the enhancement of the majority carriers' mobility in thin bodies and NWs is not related to the screening effect but rather to the complex interplay between the lateral confinement and the impurity well [42].

It is noticed that the mobility limitation in JLFETs, as in heavily doped accumulation devices is in majority governed by the dopant Coulomb scattering while the two left mechanisms, namely the phonon and surface roughness scattering have a minor impact [30, 40]. Indeed, the extracted mobility as a function of the temperature variation clearly shows a weak

impact of the phonon scattering. In contrast with an IM device where the effective mobility drops by 36 % for 200 °C temperature increase, less of 7 % of decrease is observed for the JLFET [30]. Furthermore, as the transport below the accumulation regime occurs mainly in the body center, surface roughness scattering has no tangible effect on the mobility. Also, the bulk carriers does not suffer from the Coulomb scattering induced by the potential of the oxide and interface states charges.

5.3. HCD simulation framework

In the aim of investigating the HCD on both JL and IM VSG-MOSFETs, the comparison is carried out between the two devices of the same dimensions and in the same conditions. In following table, we recapitulate the different parameters used for the simulation [43].

Table 5.1 – Main simulation parameter values used for our numerical investigation.

Parameters	JL	IM
L (nm)	30-50	30-50
T_{si} (nm)	10	10
t_{ox} (nm)	2	2
$N_{D/S}$ (cm^{-3})	$1x10^{19}$	10^{20}
N_{Ch} (cm^{-3})	$1x10^{19}$	10^{17}
Φ_m (eV)	4.88	4.63

Regarding the physical models, these latter were chosen in order to reflect the important mobility behavior in both devices. Therefore, the Klaassen mobility model which accounts for the different scattering mechanisms is incorporated. This model includes also the electric field and doping dependent mobility. Furthermore, the Shirahata mobility model which takes into account the inversion layer screening effect is combined with the previous model. As the JL body is heavily doped, the band gap narrowing is considered. Besides, Fermi-Dirac statistics are used for both devices. More effects have been activated in the simulation of

the HCD to take into account additional phenomena such as the hot electron injection, hot electron transport and the impact ionization.

The next figure illustrates the simulated transfer characteristic of both devices. It is noticed that the JL gate workfunction was chosen in order to match the off-current of the IMFET. The JLFET configuration yields a good switching property with acceptable on-state current. In comparison with the IM device where the achieved I_{on}/I_{off} ratio (@ V_{gs} = V_{ds} + V_{off}, V_{off} = V_{gs} @ I_{off} = 10 pA) and the SS are respectively 5.3x10^5 and 60.05 mV/dec, the JLFET achieved 1.7x10^5 and 60.25 mV/dec.

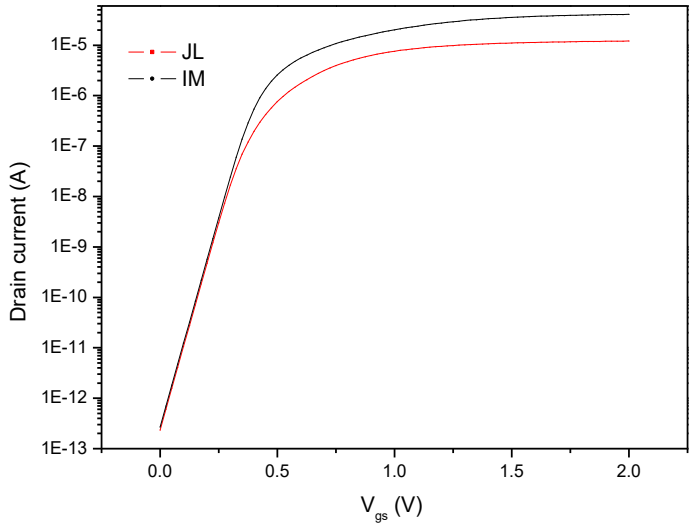

Figure 5.1 – Transfer characteristic of a JL and an IM VSG MOSFET for V_{ds}= 0.5 V.

The surface and center channel mobility variation with respect to the gate supply is depicted in fig 5.2. In the case of the IM device, both surface and body center mobility remains relatively constant during subthreshold regime. As the gate voltage is increased, the mobility degrades with the enhanced transverse electrical field and the formation of the inversion layer. The screening effect is perceptible only for low gate voltages. As the inversion layer is totally formed above the threshold voltage, the combination of the increasing scattering and transverse electric field degrades further the surface mobility that falls below of that the JLFET.

Regarding the JL case and as previously explained, the reduction of the transverse electric field associated with the screening of the Coulomb scattering improves significantly the mobility. In the channel center, the mobility improvement is principally due to the low electric field rather to any screening effect. μ_c increases with respect to the gate bias exceeding the bulk mobility which is 108 cm^2/Vs for the present doping concentration. Furthermore, the surface mobility follows the same increasing tendency as a result of the enhancement of the accumulation layer screening effect. The highest value is reached above the flatband condition. In these simulations, the surface mobility attained a maximum of 192 cm^2/Vs exceeding the IM surface mobility which is 180 cm^2/Vs at the same voltage. Nevertheless, this surface mobility improvement will have a tangible effect only if the conduction path is extended to the whole channel volume. Above this peak, the enhancement of the surface scattering with the increase of the accumulation layer density degrades the surface mobility. The resulting current limitation and low transconductance suggest that the JLFET operation in accumulation regime may be not recommended [16].

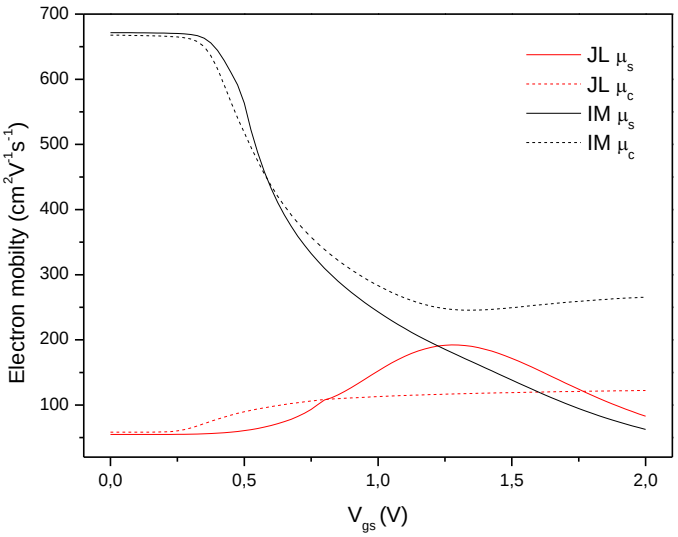

Figure 5.2 – Electron mobility in the mid-channel at the surface (line) and body center (dashed) as a function of the gate bias for JL and IM VSG-FET.

5.4. Interface trap creation process

Hot carrier effect is believed to be one of the most important causes of MOSFETs performance degradation. In n-type SOI devices, two mechanisms are identified, channel hot electron and hot electron injection through the oxide layer. In the first mechanism, the accelerated carriers acquire enough kinetic energy to break silicon bonds. If the interface is beforehand H-passivated, the hot electrons will depassivate the Si-H bond by collision in a single or multi particle process [44]. The resulting dangling bonds act as interface states that can capture the channel electrons or reemitting them into the latter. Also, the predominance of the CHE on the interface traps generation was demonstrated. This conclusion was made by the analysis of the generated deuterium by CHE and HCI. It was found that large deuterium isotope generation is observed in the presence of CHE, resulting in higher interface trap density [6].

However, in this work, we consider only the HCI as the main process responsible of the interface traps creation. Although it was proved nowadays that this widely accepted concept is physically incomplete, especially in submicron scale, it provides acceptable description of the HCD [3-5]. The common model supposes that the hot electron can be injected into the oxide if it gains sufficient energy to surmount the Si-SiO_2 interface barrier evaluated at 3.2 eV [3]. Once the electron crosses the interface barrier, it can result either on interface state creation or be trapped in the oxide.

Moreover, the prevalence of the interface states on the oxide traps generation depends on the stress bias conditions. It was demonstrated that the interface states generation is predominant for $V_g \approx V_d/2$. The reverse situation is observed for $V_g \approx V_d$ [5, 7]. Furthermore, the injection of the impact ionization and avalanche multiplication excess carrier increase further the interface and oxide trap creation [1].

In the simulation framework, the Hänsch reliability model is used to generate the HCD [4, 43]. The interface trap creation is calculated basing on (5.1), where N_{acc}^{0} represents the initial acceptor like traps density, σ_e is the electron capture cross section and $N(x,t)$ is the time and position dependent traps. It is noticed that only the acceptor like traps are considered with an initial density of 5×10^{12} cm^{-2}, uniformly distributed over the silicon/oxide interface, which is coherent with the experimental reported data for both device types [45,

46]. $J_{inj,n}$ represents the HEI current density based on the Tam lucky electron model [3, 43]. It is assumed that only HEI occurs under the present DC stress conditions, namely V_{ds} = 3 V and V_{gs} = 1.5 V. Also, it is noticed that this bias conditions are exaggerated in order to amplify the degradation and reduce the simulation time, it was reported in literature that the power supply for 10 years lifetime of JL and IM nanowire structures varies around 1.5 V [14]. Furthermore, the interface traps recovery is neglected, as well as the oxide trapping/detrapping process and the fixed oxide charge.

$$\frac{dN(x,t)}{dt} = \frac{\sigma_e}{q} J_{inj,n}(x,t)(N_{acc}^0(x) - N(x,t)) \tag{5.1}$$

The probability that an electron gain sufficient energy to surmount the local barrier and create an interface trap depends essentially on the electric field and the surface carrier density. As these latter are more important in IM than in JL device, the injected current follows the same trend as depicted in fig 5.3. Consequently, the interface trap generation reaches greater densities in the IM than in the JL. Approximately, the total interface trap charge is 1.5 times greater in the former device (fig 5.4).

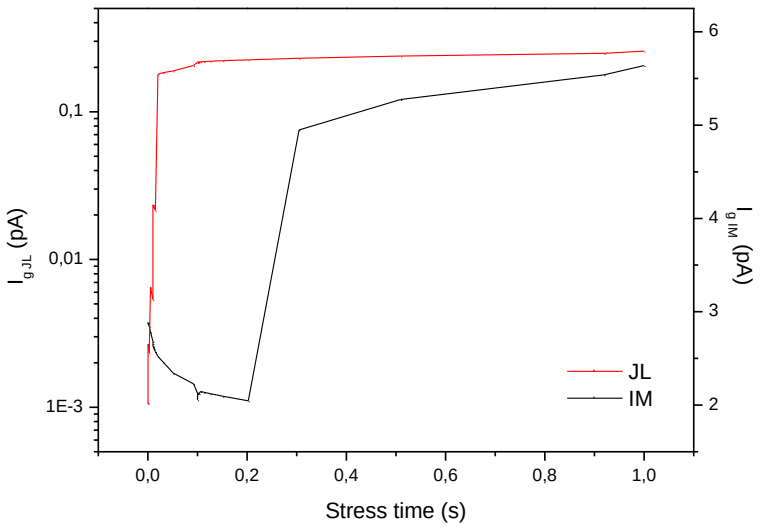

Figure 5.3 – Gate leakage current as a function of stress time.

The effect of the impact ionization on the interface traps creation is also depicted in the next figure. It is shown that in a first period, the excess carrier generated by II at the drain junction of the IM device results in an enhancement of the interface states creation. With extended stress time, the enhanced trapped electron charge lead to the reduction of the electric field and carrier density at the interface. Consequently, the second period of the HCD exhibits a decrease of the II process as well as the traps creation that starts to saturate.

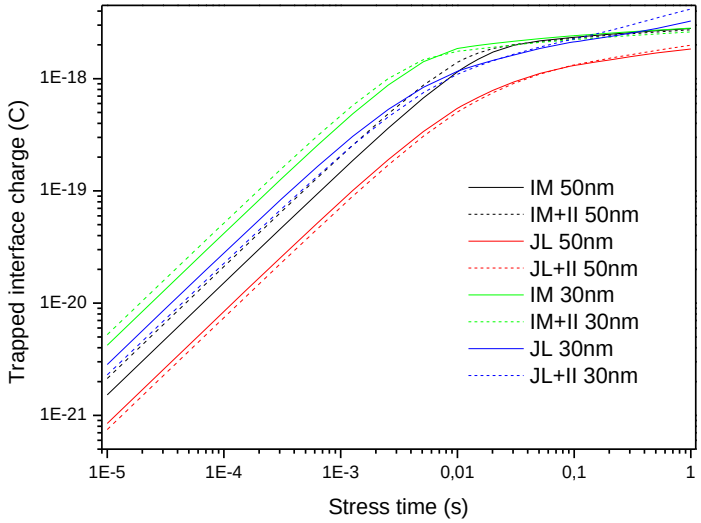

Figure 5.4 – Trapped interface electron charge as a function of stress time.

The JLFET on the other hand exhibits a reverse behavior. As previously mentioned, the II process occurs mainly into the drain extension. Therefore, the generated electrons are evacuated toward the drain contact and have small impact on the gated interface. These electrons would be implicated in the creation of interface traps if oxide spacers are considered which is not the case in this study. Furthermore, the generated holes are injected in the channel where they recombine. Therefore, the channel carrier density decreases resulting in less interface traps creation in a first period. In a second time however, the enlargement of the interface traps distribution attenuates the II generation resulting in less carrier recombination in the channel and high interface carrier densities. An enhancement of the electric field is also observed, particularly the perpendicular

component beneath the damaged interface. Hence, the interface states creation as well as the trapped electron charge keep increasing as depicted in fig 5.4.

Considering the HCD on shorter channels, a significant enhancement of the interface traps creation is observed in the two types of device, as a result of the electric field increase, resulting in larger degradation and reduction of the devices lifetime as experimentally reported in [14]. A more pronounced enhancement of the II effect is noticed in the case of the JLFET. This fact can be explained by the reduction of carriers' recombination in shorter channels, larger part of the generated holes reach the source before recombining maintaining the interface carrier density at high levels. It also noticed that the trapped interface charge of the IM device reaches approximately the same levels of saturation while for the JLFET, the same ratio between the linear and saturation region is observed. This fact can be explained by exploring the temporal evolution of the interface traps distribution over the gate length in both devices as illustrated in the following figures.

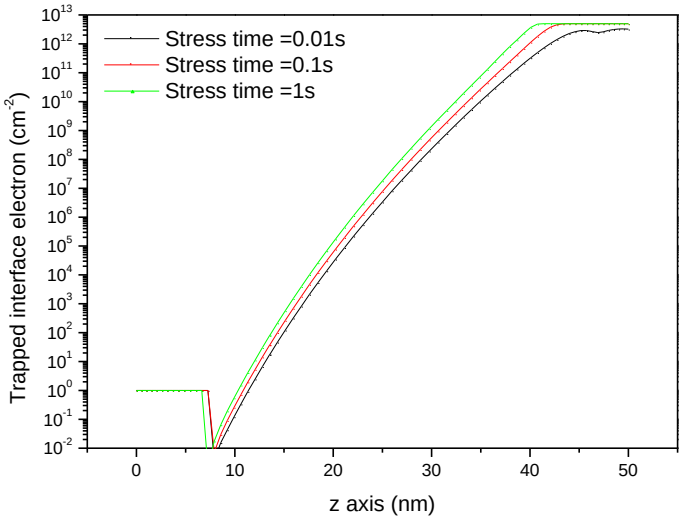

Figure 5.5 – Trapped interface electron distribution for 50 nm IM device.

Indeed, the performed simulations on the two types of device with 50 nm of gate length highlight a particular profile for each type. It appears that this specific interface traps distribution is elevated with extended stress time. When reaching the maximum allowable interface states density, the profile saturates and exhibits an extension toward the source

[44]. Furthermore, the enhanced HCD in IMFET is clearly depicted in fig 5.5 with a larger saturated damaged region. The enhanced trapped interface charge of the JL device can also be explained by the increase of the interface traps densities in the remaining channel interface as shown in fig 5.6.

Usually, the interface traps are limited to the drain side over a fixed length neglecting the remaining interface. This approach results in misleading degradation of devices' properties. Even if the interface state density decrease while receding from the drain junction, their impact on the surface potential and the electric field must be taken into account, especially for densities above 10^{10} cm^{-2}.

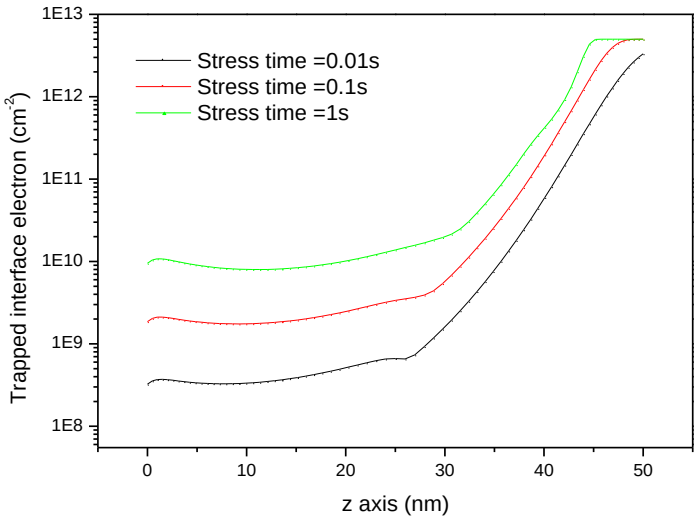

Figure 5.6 – Trapped interface electron distribution for 50 nm JL device.

5.5. HCD of device's performances

In this section, an assessment of the hot carrier effect on the device properties is performed. For this aim, the previous extracted interface traps distribution from the HCD simulation on IM VSG-MOSFET is used for both types of device, rather to vary the traps density over a fixed length as usually used. Furthermore, the amphoteric property and density of state of interface traps is considered. In this manner, a more realistic behavior is obtained. It is noticed that only acceptor like interface traps are considered as the donor like

traps yield small variation of the IM device properties and negligible on the JLFET. The amphoteric property of an acceptor like interface trap means that this latter act as negatively charged state when filled and neutral when empty. The level of traps filling depends on the channel Fermi level position with respect to traps energy distribution. Thus, a dynamic response of the interface states is obtained for the different operating regime conversely to the static fixed oxide charge.

The interface states energy distribution depends on many factors. Indeed, the energy distribution of interface states in ultrathin oxide layer was found to be dependent on the nature of the dangling bond (either it interact with Si or O atoms) and the temperature of the oxide layer formation. For instance, only one energy peak in the midgap was observed for 350 °C with ~0.1 eV width, while 2 peaks were detected for temperatures above 550°C [47]. A correlation between the paramagnetic centers P_b (which are dangling bonds) and the interface states density was previously demonstrated [45]. It was found that this type of interface traps depends on the Si/SiO_2 interface orientation. Indeed, only one P_b center appears in (111) interface yielding a U shape density profile [48]. In (100) interface orientation, two centers are observed, P_{b0} and P_{b1}. The P_{b0} centers represent the dominant part of the DOS, they are well centered in each half of the bandgap. The P_{b1} yields lower traps density and are located near the mid-gap [49]. Also, higher interface traps density was measured for n-type doping [45]. Moreover, the oxide material, thickness, body doping concentration and characterization methods result in different interface states energy distributions [46, 50].

Without a real consensus, an arbitrary large gaussian distribution of interface traps DOS is incorporated with a peak energy/peak distribution of 0.49 eV from the silicon conduction band and characteristic decay energy of 0.2 eV. The peak distribution is increased from 10^{12} to a maximum of 10^{13} which corresponds to the first phase of interface trap creation. The saturation phase is described by the enlargement of the peak distribution length toward the source.

Fig 5.7 illustrates the drain current degradation for both JL and IM devices. It is noticed that the interface trap density in the remaining of this study corresponds to the distribution mean value computed by $1/L\int_0^L N_{it}(z)dz$. The obtained results corroborate the reported

HCD on IM devices [5, 51]. It is shown that the degradation of transfer characteristic occurs mainly during the depletion and weak inversion regime. In fact, the negatively charged traps lead to an elevation of the channel barrier which reduces further the subthreshold current and delays the device onset. As the gate voltage increases, the formation of the inversion layer causes a bending of the channel conduction band at the interface. Consequently, the Fermi level with respect to the traps energy level is modified increasing therefore the interface charge. The impact of the interface states on the JL is very similar, the degradation being relevant during full and partial depletion. The negative charge behavior is expected to be at its maximum during full depletion as the band profile at the interface yields the maximum traps filling. The effect decreases progressively as the device switches to partial depletion and almost vanishes above the flatband condition.

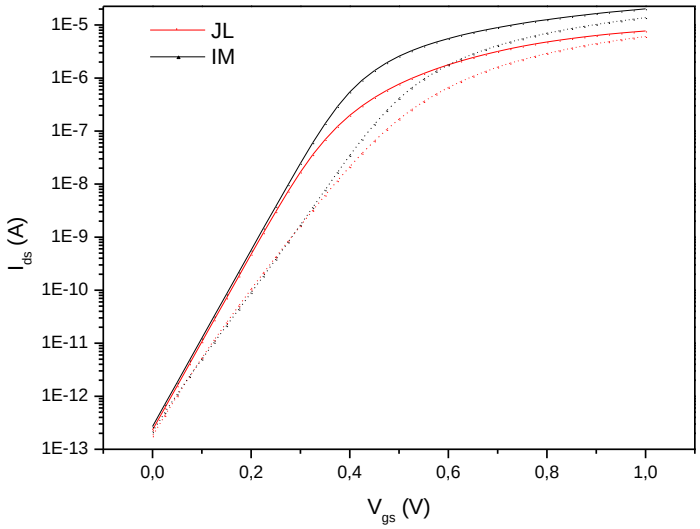

Figure 5.7 – Drain current for (line) fresh and (dot) damaged JL and IM VSG FET with L=50 nm, V_{ds}=0.5 V, N_{it}=7,9E11 cm^{-2}.

Fig 5.8 illustrates the impact of interface states density enhancement on the subthreshold slope degradation of the two types of device. It is shown that the IM device exhibits a relative stability in the presence of low traps densities. As the density increases and get deeper in channel, the impact on the barrier elevation is enlarged yielding major

subthreshold degradation. On the other hand, a moderate impact of the interface states on the JL device in comparison with its IM counterpart is observed.

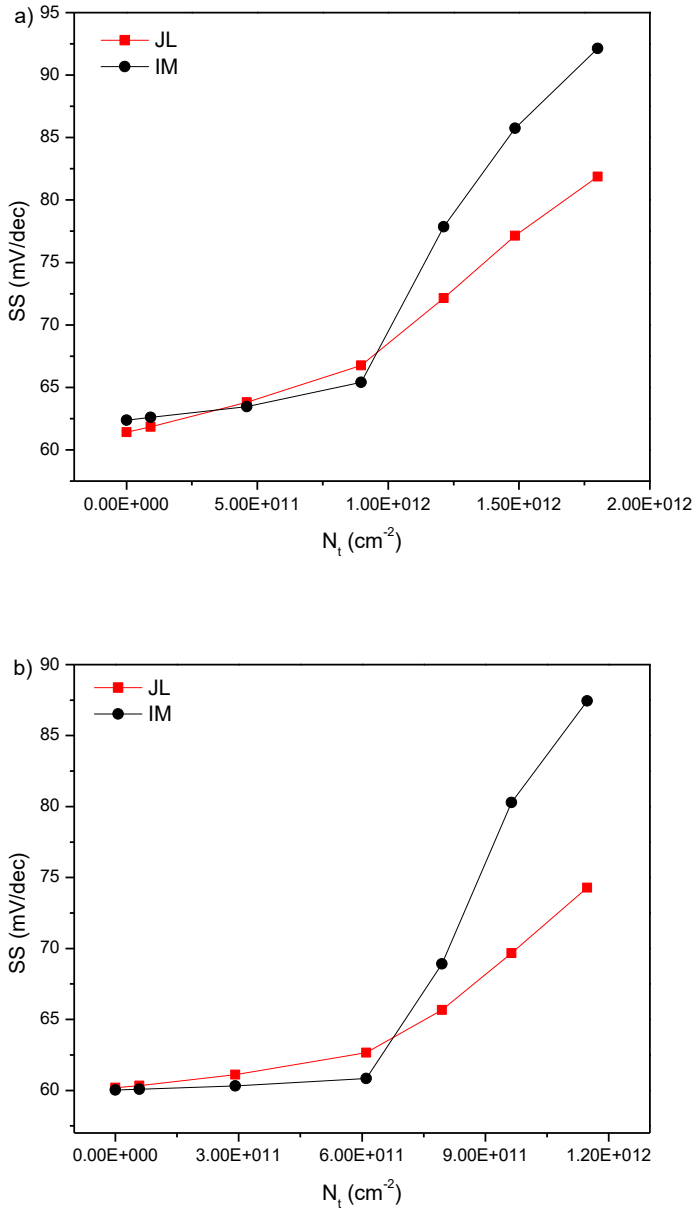

Figure 5.8 – Subthreshold slope degradation for JL and IM VSG FET for (a) L=30 nm, (b) L=50 nm, V_{ds}=0.5 V.

This relatively low degradation is mainly due to the location of the conduction path. It is clear that the bulk conduction mode is less affected by the interface charge than the surface conduction mode. As the interface states distribution increases, a deeper and larger

depletion area is formed which delays the creation of the conduction path. The JL device immunity against SCEs is also observed in fig 5.8a yielding lower SS for fresh devices. The degradation follows the same evolution as for longer channel length. However, relatively larger degradation is reached.

The channel potential shift induced by the charged interface states yields a sensible variation of the threshold voltage as depicted in fig 5.9. The extraction was made using the maximum transconductance derivative method.

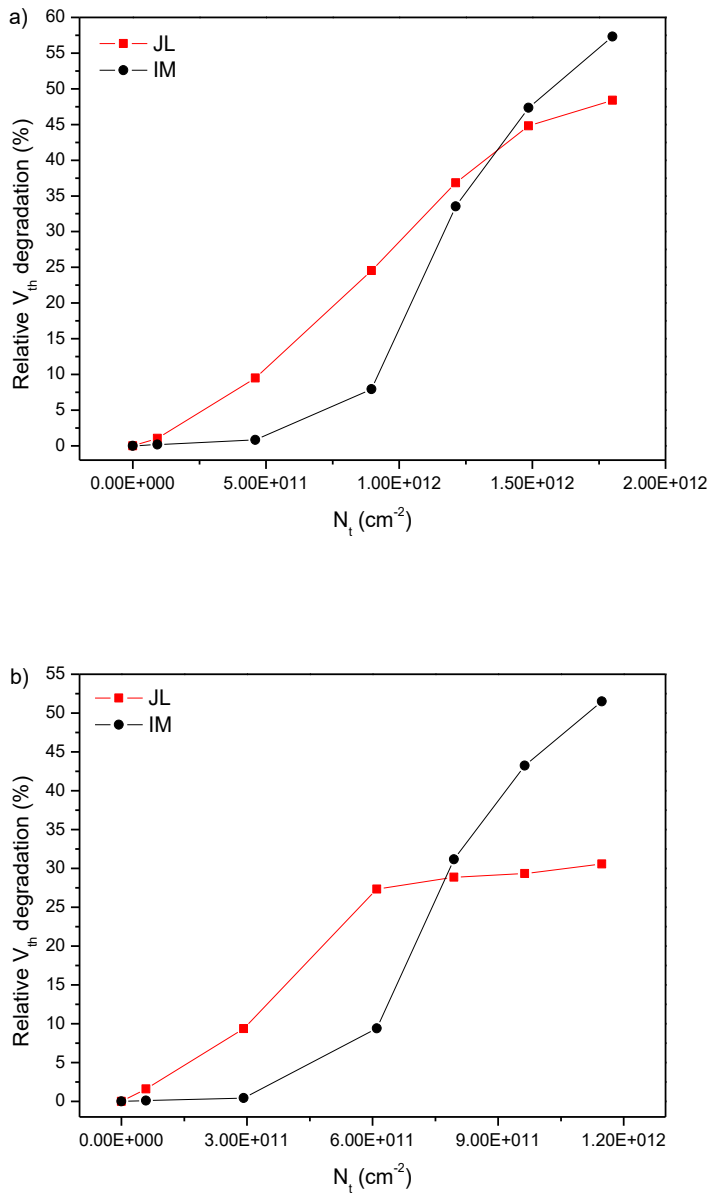

Figure 5.9 – Relative threshold voltage degradation for JL and IM VSG FET for (a) L=30 nm, (b) L=50 nm, V_{ds}=0.5 V.

It appears that the IM device V_{th} shifts gradually for low interface traps densities and increases in an exponential manner for higher values. For the JL device, the relative degradation increases quasi linearly with interface traps density raise. However, an attenuation is observed for high densities suggesting that the degradation might reach a saturation level with longer aging phenomenon. Furthermore, larger V_{th} variation is observed for shorter channel length. The degradation for 30 nm JLFET reaches 50 %, while for 50 nm, it does not exceeds the 30 %. Conversely, high degradation is observed in the case of IM device for both channel lengths. Overall, for low and moderate interface states densities, the IMFET exhibits much lower V_{th} degradation in comparison with it JL counterpart. Nevertheless, this tendency is reversed with for high traps densities.

The on-current variation and its relative degradation are depicted in fig 5.10. A quasi-linear degradation is observed for the JL device while for the IM type, the degradation evolves linearly for low traps densities and increases with the enlarging of the interface states distribution. The I_{on} is measured for 1 V of gate bias. At this bias condition, the IM device is in strong inversion and the JL device is in partial depletion regime. The amount of trapped electrons in the acceptor-like interface states is more relevant in the JL device yielding larger interface charge. Nevertheless, the difference in the conduction path location leads to different impact of interface charge on the carrier transport. It is clear that the inversion layer, by its position is more affected by the interface states, especially for high densities and thus despite the lower trapped charge. Although a small improvement of the current is observed for shorter length, the relative degradation reaches approximately the same levels for both types of device.

The large IMFET current degradation can also be attributed to the enhancement of the Coulomb scattering due to the local potential of the charged states [2]. It is clear that this additional scattering causes a degradation of the surface mobility and has no direct impact on the carrier transport in the channel center. Simulations show that the presence of interface traps results in the shift and lowering of the effective mobility peak as depicted in fig 5.11. The Coulomb scattering being dominant for low carrier's density, i.e. low gate bias, the impact of interface traps on the effective mobility is observable only for weak inversion (for IM device) and partial depletion (for JL device). The effective mobility was extracted using the following definition [39]:

$$\mu_{eff} = \frac{LI_d(V_g)}{qn_s(V_g)V_dW} = \frac{L^2 I_d(V_g)}{V_d \int C_g(V_g)dV_g} \quad (5.2)$$

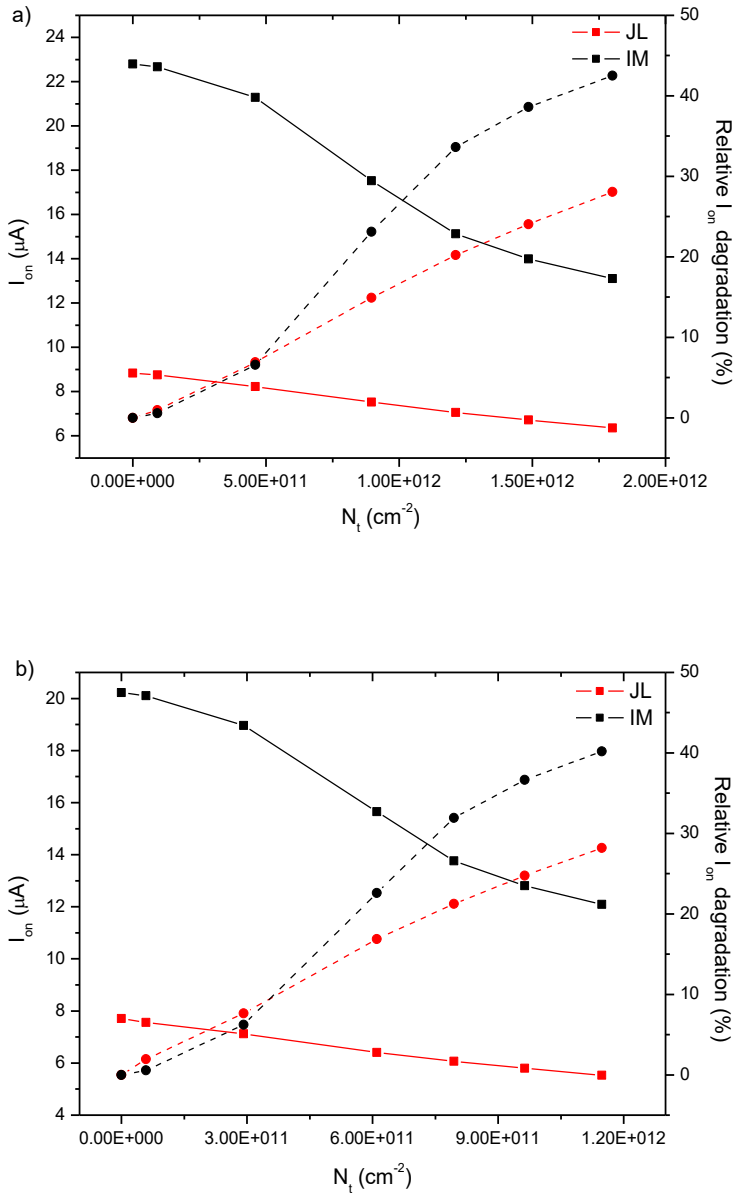

Figure 5.10 – I_{on} (line) and relative I_{on} degradation (dashed) for JL and IM VSG FET for (a) L=30 nm, (b) L=50 nm, V_{ds}=0.5 V, V_{gs}=1 V.

where n_s is sheet density of mobile carriers in the channel evaluated by integration of the total gate capacitance C_g extracted from C-V curves. V_{ds} was set at 0.01 V to eliminate the

effect of high lateral electric field. Fig 5.12 shows the maximum effective mobility degradation as a function of the interface states density.

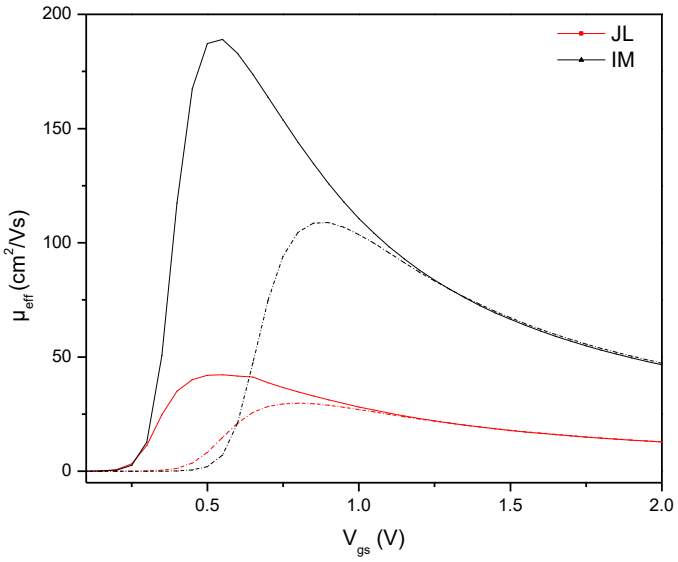

Figure 5.11 – Effective mobility as a function of the gate bias for (line) fresh, (dashed) damaged JL and IM VSG FET with L=50 nm, V_{ds}=0.01 V.

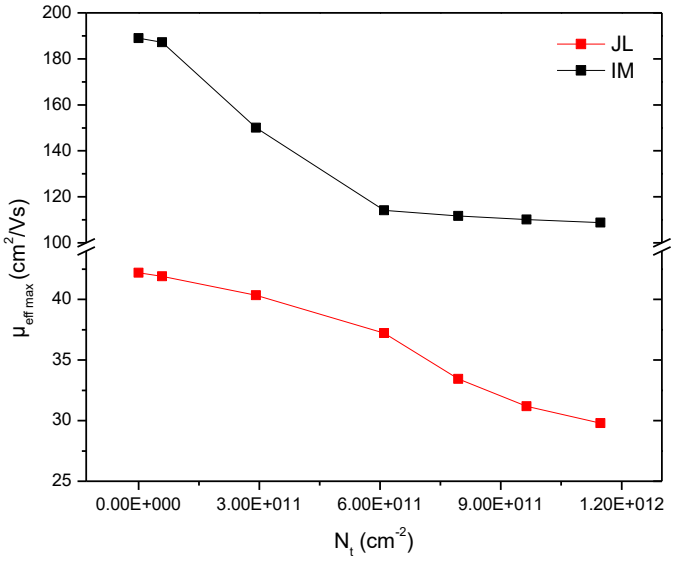

Figure 5.12 – Maximum effective mobility degradation with respect to N_{it} for JL and IM VSG FET with L=50 nm, V_{ds}=0.01 V.

As it is expected, a major degradation of the IM effective mobility that exceeds 40% is observed. The JL device on the other hand exhibits much lower degradation that reaches 20%. It is believed that this degradation is not related to the Coulomb scattering of the interface states but rather to the perpendicular electric field enhancement.

The shift in the transfer characteristic yields also relative transconductance decrease. Similarly to the drain current, a linear degradation of the transconductance is observed in the case of the JL device (fig 5.14). The IM type on the other hand, exhibits small variation for low traps densities and much lower relative degradation in comparison with the JL device. As the interface states density extends toward the source, major degradation of the transconductance is observed, attaining the JLFET values. Relatively, the degradation approaches the 100 % and largely exceeds its JL counterpart. This tremendous degradation of the IM device can be attributed to the same reasons of the drain current degradation, i.e. the enhanced effect of the charged interface states on the conduction path and surface mobility. Although sensible improvement of the transconductance results from the channel length reduction for both types of device (fig 5.14a), the same degradation evolution is observed for both lengths.

Fig 5.15 illustrates the intrinsic gain degradation for JL and IM devices. It is shown that the gain of a fresh IM device reaches twice its JL counterpart. Furthermore, the length reduction divides the gain by 2, which shows a large improvement of the output conductance. Consequently to the transconductance dropping in the presence of interface states, the intrinsic gain degrades as well. However, an improvement of the gain is observed above a certain amount of interface traps density. This is due to the increased degradation of the output conductance for longer aging phenomenon. Furthermore, the fact that the transconductance degradation is less important in JL device results in better improvement of the intrinsic gain that exceeds its IM counterpart.

Regarding the unity gain cutoff frequency (fig 5.16), simulations show acceptable values for the JL device exceeding the half of the fresh IM value. Furthermore, the channel length reduction by 20 nm yields better improvement of the JLFET cutoff frequency. As for the previous parameters, the IM exhibits moderate cutoff frequency degradation for low interface traps densities. However, the extended HCD yields tremendous degradation that approaches 100 % and falls above the JLFET value for 30 nm gate length. In the case of JL

device, a quasi linear degradation is observed. A sensible attenuation is observed for higher interface states densities which can be attributed to the degradation of the total gate capacitance accentuated by the increasing interface charge.

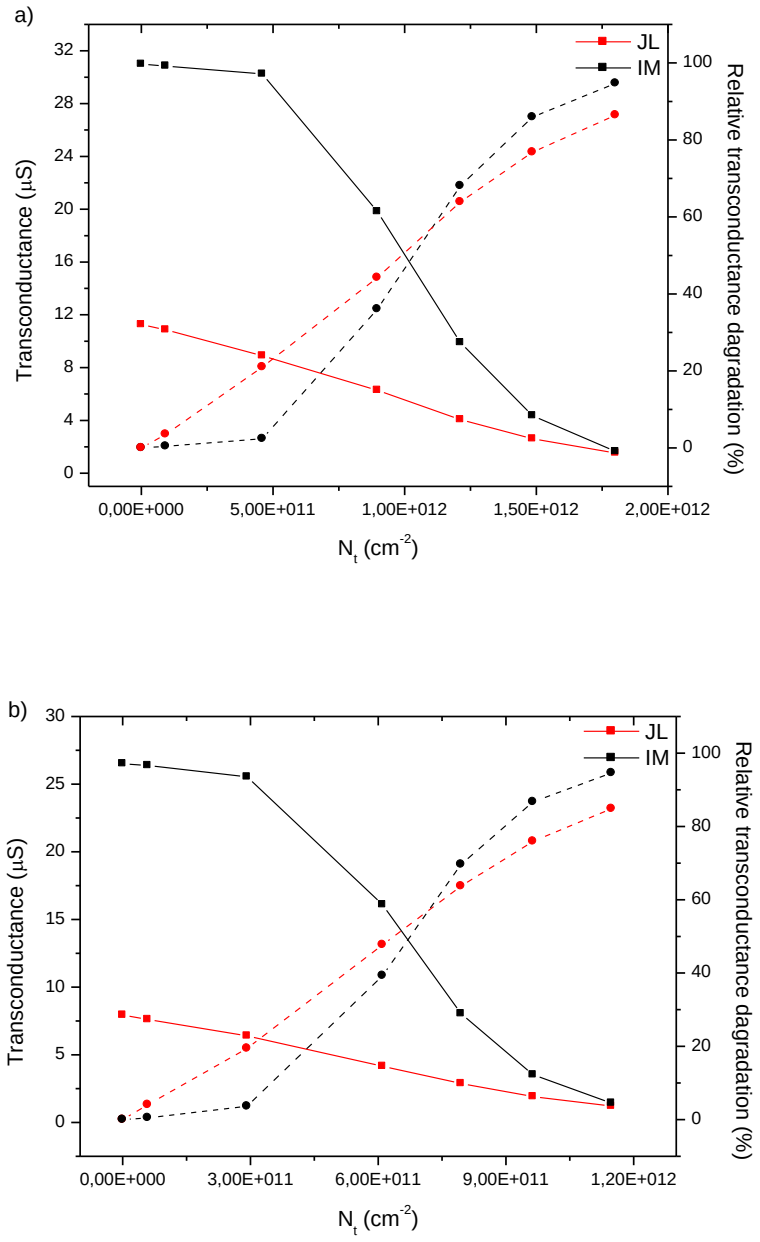

Figure 5.14 – G_m (line) and relative G_m degradation (dashed) for JL and IM VSG FET for (a) L=30 nm, (b) L=50 nm, V_{ds}=0.5 V, V_{gs}=0.5 V.

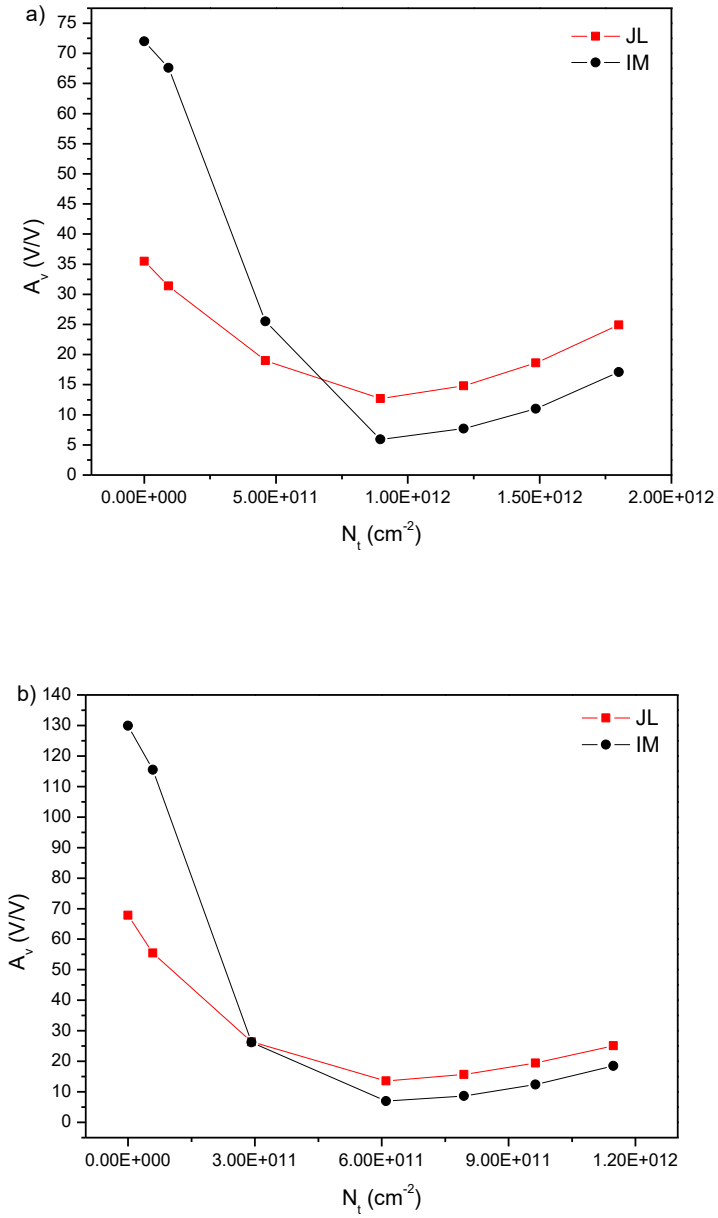

Figure 5.15 – Intrinsic gain degradation for JL and IM VSG FET for (a) L=30 nm, (b) L = 50 nm, V_{ds}= 0.5 V, V_{gs} = 0.5 V.

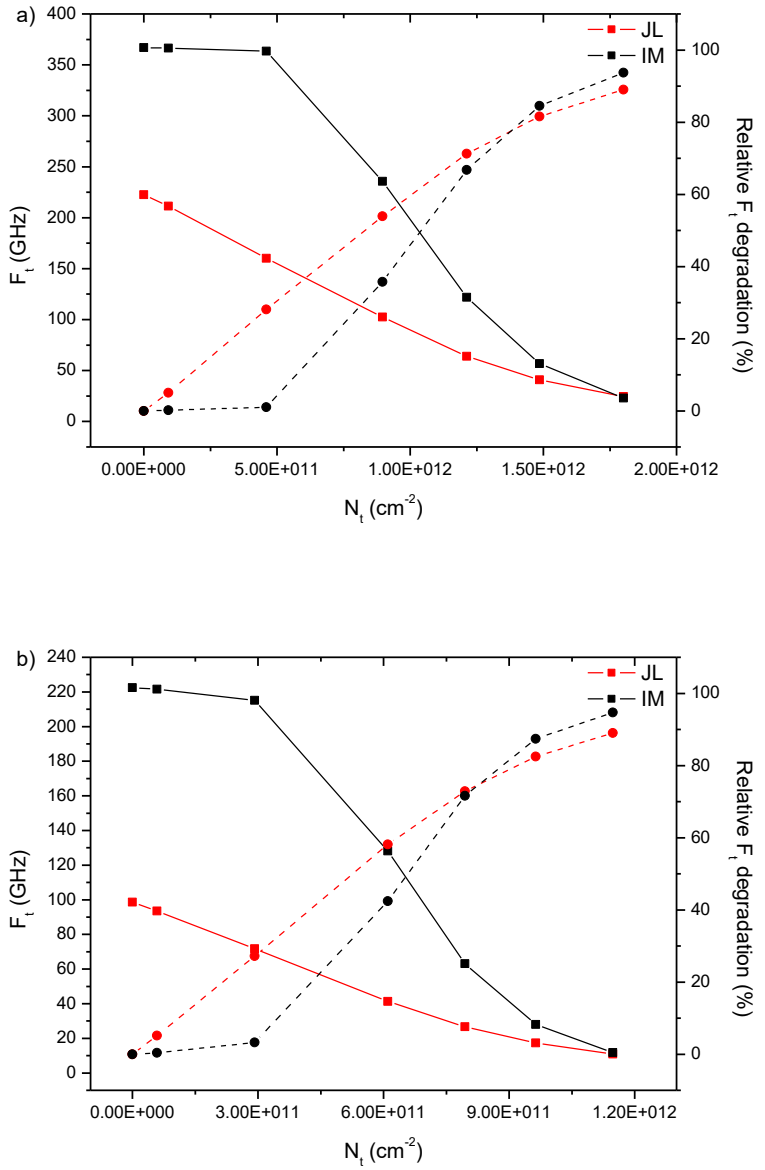

Figure 5.16 – Cutoff frequency (line) and its relative degradation (dashed) for JL and IM VSG FET for (a) L=30 nm, (b) L=50 nm, V_{ds}=0.5 V, V_{gs}=0.5 V.

Summarizing the previous results, it appears that the HCD will be very harmful for the both devices' operation either in analog/RF or digital application. Considering analog/RF application, the drain current and transconductance degradation will reduce the upper limit of the operating range. Signal distortion, compression/extension and corruption might also occur. In amplifiers, the gain degradation will lead to a loss of the original circuit performances. The cutoff frequency dropping will reduce the bandwidth which can be

problematic for radiofrequency transceiver. If the inversion mode device exhibits a relative stability for low interface traps densities, the reveled major degradations for higher densities suggests that the junctionless transistor will have a better resilience to longer aging phenomenon. The impact of HCD on digital applications is discussed in the next section.

5.6. HCD in digital application

5.6.1. Static analysis

In this section, the impact of HCD on CMOS inverter operation is considered. The degradation of the conception keys that are the threshold voltage and the transconductance implies a deterioration of the inverter properties. Fig 5.17 illustrates the voltage transfer characteristic (VTC) of a fully functional complementary JLFET based inverter. The p-type JL is identical to the n-type with a channel doping of 2.5x10^{19} cm^{-3} and a gate workfunction of 4.26 eV, the latter are chosen in order to obtain a switching threshold of $V_{dd}/2$ (V_{dd}=1 V).

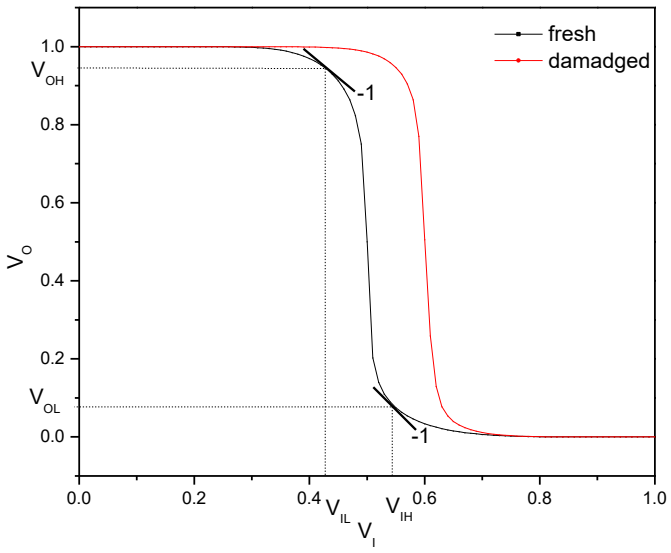

Figure 5.17 – VTC of 50 nm VSG-JL based inverter for fresh and damaged n-type device (N_{it}=7,9E11 cm^{-2}).

The noise margin (NM) is a key feature of logic application design. Largest NM values ensures correct circuit operation and stability against signal noise that may lead to a bit reversal in cascade configuration [52]. The NM for the two inverter states are defined as, $NM_H=V_{OH}-V_{IH}$ and $NM_L=V_{IL}-V_{OL}$. $V_{I,O/L,H}$ are the operational points and correspond to a voltage gain of -1. For fresh devices, the JL inverter achieved large noise margins with NM_H= 390 mV and NM_L= 359 mV. On the other hand, the IM inverter achieved NM_H= 403 mV and NM_L= 340mV.

As shown in the previous figure, the presence of interface states in the n-type device yields a shift toward the right of the output voltage and the switching threshold. Consequently, the high noise margin decreases with a relative increase of the low noise margin. Considering the worst case (i.e. the lowest NM), the NM_H degradation is depicted in fig 5.18. For low interface traps densities, the degradation follows the same profile for both types of device with relative higher values for the JL based inverter. As the traps density is further increased, the relative NM degradation of the IM based inverter exceeds that of the JL type yielding NM values lower for the former circuit than for the latter.

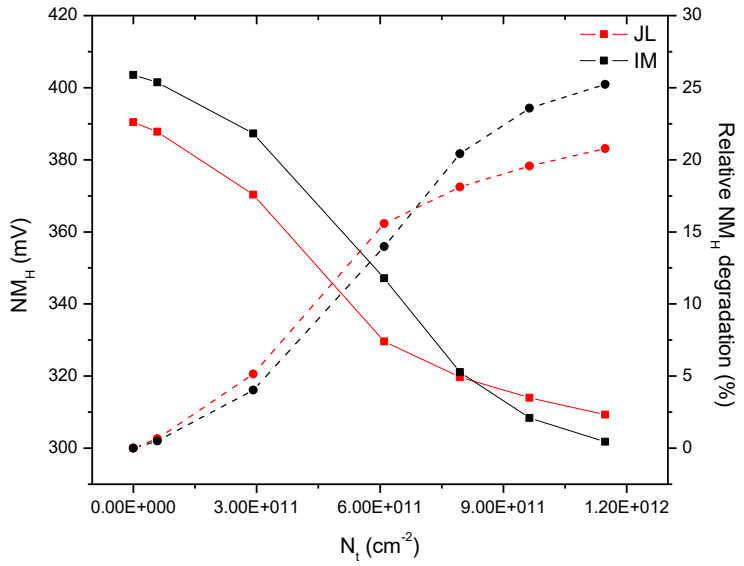

Figure 5.18 – NM_H (line) and relative NM_H degradation (dashed) for VSG-JL and IM based inverter.

5.6.2. Transient analysis

The next figure shows the transient response of VSG-JL and IM based inverter. The output is lumped with an external capacitance of 2 fF for the IM based inverter. Because of the large equivalent resistance (lower saturation current) and C_{gd} of the JLFET, the external capacitance is set to 0.2 fF in order to obtain rise and fall times close to those yielded by IMFETs. It is noticed that the oxide capacitance is evaluated at 34 aF for both devices. However, the total internal capacitance is lower in the JLFET due to the absence of junction capacitances. Simulations show an increase of the fall time of the damaged device based inverter. This increase results from the degradation of many parameters such as the transconductance, drain current and capacitance. Despite the fact that the trapped electrons yields a negative charge that decreases the C_{gd} during saturation, the impact of the drain current degradation on the discharging time is more relevant. On the other hand, the rise time remains unaffected as it depends essentially on the p-type transistor characteristics.

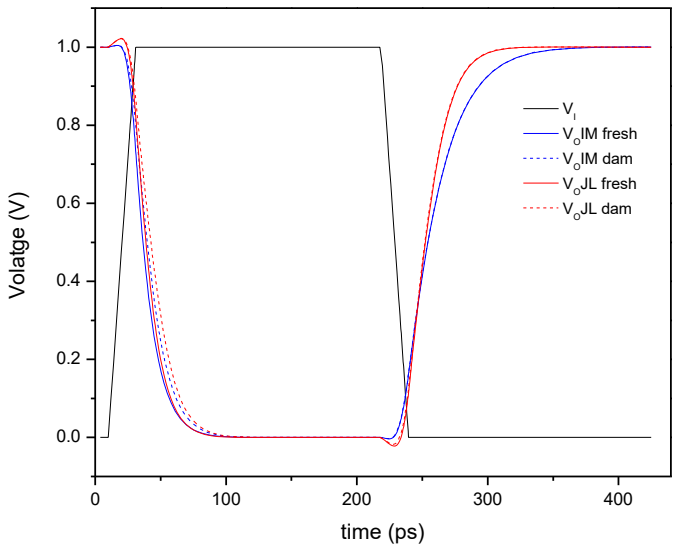

Figure 5.19 – Transient response of fresh and damaged VSG-JL and IM based inverter.

The degradation of the propagation delay is illustrated in fig 5.20. It is defined as $\tau_p = (\tau_{pH} + \tau_{pL})/2$, where τ_{pH} and τ_{pL} are respectively the high-to-low and low-to-high

transition propagation delays that reflect the elapsed time for the output to reach 50 % of V_{dd} with respect to the input voltage at same level. As expected from the large equivalent resistance of the JLFET, relatively longer propagation delay and higher relative degradation are obtained. The degradation for both devices follows the same increasing profile. Nevertheless, the difference between tends to decrease with extended stress time.

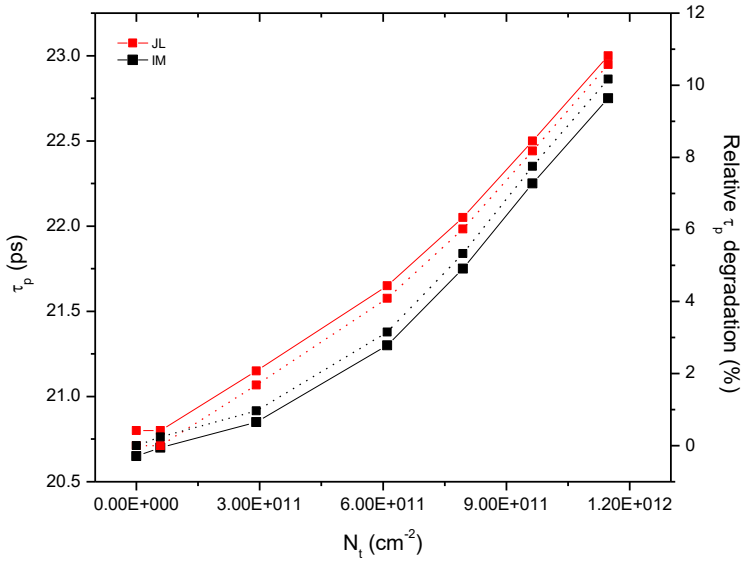

Figure 5.20 – τ_p (line) and relative τ_p degradation (dashed) for VSG-JL and IM based inverter.

Moreover, the transient analysis reveals an amplification of the over/undershoots voltages peaks. These peaks are inherent to the inverter operation and result from the coupling of the input ramp to the output while the change in the transistors states has not started yet. The coupling occurs via the C_{gd} (Miller capacitance) of the two transistors. Also, the over/undershooting time adds up to the transition one resulting in the enhancement of the propagation delay and power dissipation. In the next figure, the overshoot voltage V_{ov} is extracted for various interface states densities of both JL and IM based inverter. For fresh JLFET, V_{ov} is almost 5 times higher than its IM counterpart. This large value results from the lower C_L as the peak voltage can be computed by $V_{ov}= V_{dd}\times C_M/(C_{M+}C_L)$ [53]. Considering the relative degradation of V_{ov}, better values are observed for the IM based inverter for low interface traps densities. This tendency reverses with longer aging phenomenon attaining more than 2 times the relative degradation of the JLFET based circuit.

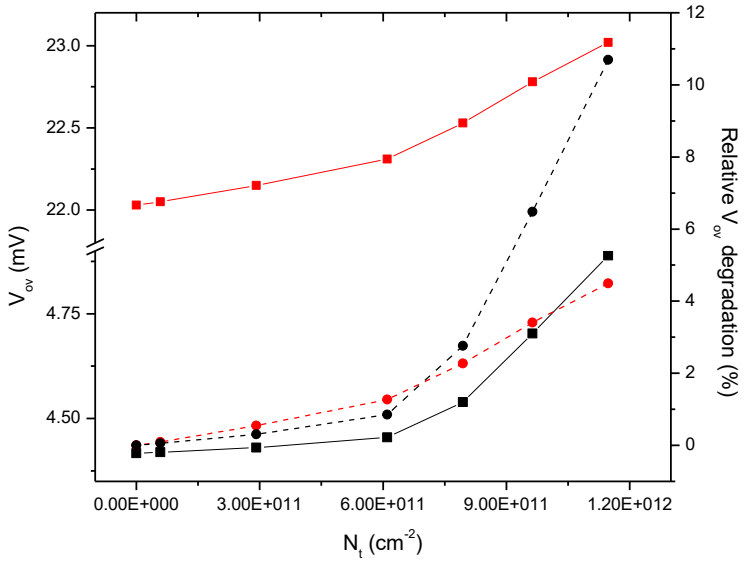

Figure 5.21 – V_{ov} (line) and relative V_{ov} degradation (dashed) for VSG-JL and IM based inverter.

Overall, the carried out simulations show that the inverter based on the two types of device still has its total functionality after a long aging process even if it loses its symmetry. In a single stage, the parameters degradation will essentially increase the total power dissipation. For cascade topologies such as ring oscillators, the propagation delay degradation will result in a decrease of the oscillation frequency. The results highlighted also the better resilience of the JLFET based inverter for longer aging process.

5.7. Conclusion

In this chapter, a comparative study of the HCD on JL and IM VSG MOSFET was proposed. The analysis focused on the interface state creation. Using the appropriate stress voltage conditions, simulations show that the created interface charge is not less than 1.5 times higher in IM device. Despite of the enhanced impact ionization in JLFETs, the continuous recombination in the channel attenuates the interface traps creation. Also, a deeper penetration into the channel of the interface states profile with respect to the stress time is observed for the IM device.

Basing on the interface traps profile evolution with stress time and their amphoteric property, a more realistic response of the interface states in the different operating regimes is obtained. An evaluation of the HCD on many electrical characteristics of the two types of device was performed. Major degradation of all the metrics in subthreshold and superthreshold regime is observed. Enhanced degradation is noticed in the IMFET for high interface states density leading in most cases to the underperformance of this device in comparison with its JL counterpart. The enhanced immunity of the JLFET against SCEs was demonstrated. For equivalent interface states densities, an improved immunity of shorter channel devices was observed. Accordingly, the combination of the lower interface traps creation and the low degradation exhibited by the JLFET demonstrates a much better immunity against HCD and confirms the longer lifetime of this device.

The assessment of HCD on both JL and IM VSG based CMOS inverter was performed. It appears that the presence of interface states yields a degradation of the majority of the circuit metrics. Nevertheless, the JLFET based inverter exhibits a better immunity against HCD. Besides elucidating the superior reliability of the JLFET at device and circuit level, this study emphasizes the importance of interface states creation and distribution for HCD evaluation. Therefore, it is necessary to develop new compact models that incorporate a more realistic description of the aging phenomenon.

References

[1] E. Takeda, Hot-carrier effects in scaled MOS devices, Microelectronics Reliability, pp. 1687-1711, vol. 33, Sep. 1993.

[2] P. Roblin, A. Samman, S. Bibyk, “Simulation of hot-electron trapping and aging of nMOSFETs,” IEEE Transactions on Electron Devices, vol. 35, pp. 2229-2237, Dec. 1988.

[3] S. Tam, P-K. Ko, C. Hu, “Lucky-electron model of channel hot-electron injection in MOSFET's,” IEEE Transactions on Electron Devices, vol. 31, pp. 1116-1125, Sep. 1984.

[4] W. Hänsch, A.V. Schwerin, F. Hofmann, “A new self-consistent modeling approach to investigating MOSFET degradation,” IEEE Electron Device Letters, vol. 11, pp. 362-364, Sep. 1990.

[5] B. Doyle, M. Bourcerie, J-C. Marchetaux, A. Boudou, “Interface State Creation and Charge Trapping in the Medium-to-High Gate Voltage Range ($V_d/2 \geq V_g \geq V_d$) During Hot-Carrier Stressing of n-MOS Transistors,” IEEE Transactions on Electron Devices, vol. 37, pp. 744-754, Mar. 1990.

[6] Z. Chen, *et al*., “On the mechanism for interface trap generation in MOS transistors due to channel hot carrier stressing,” IEEE Electron Device Letters, vol. 21, pp. 24-26, Jan. 2000.

[7] A. Bravaix, *et al*., “Hot-Carrier acceleration factors for low power management in DC-AC stressed 40nm NMOS node at high temperature,” Reliability Physics Symposium, 2009 IEEE International, Montreal, QC, Canada, 26-30 April 2009.

[8] S. Rauch, G. La Rosa, F. Guarin, “Role of e-e scattering in the enhancement of channel hot carrier degradation of deep-submicron nMOSFETs at high Vgs conditions,” IEEE Transactions on Device and Materials Reliability, vol. 1, pp. 113-119, Jun. 2001.

[9] K.N. Quader, *et al*., “Hot-carrier-reliability design guidelines for CMOS logic circuits,” IEEE Journal of Solid-State Circuits, vol. 29, pp. 253-262, Mar. 1994.

[10] http://bsim.berkeley.edu/

[11] I. Sanchez Esqueda, H. J. Barnaby, M. P. King, “Compact Modeling of Total Ionizing Dose and Aging Effects in MOS Technologies,” IEEE Transactions on Nuclear Science, vol. 62, pp. 1501-1515 , Aug. 2015.

[12] S-Y. Kim, *et al*., A Comparative Study on Hot-Carrier Injection in 5-Story Vertically Integrated Inversion-Mode and Junctionless-Mode Gate-All-Around MOSFETs, IEEE Electron Device Letters, vol. 39, pp. 4-7, Jan. 2018.

[13] S. M. Lee, J. Y. Kim, C. G. Yu, J. T. Park, "A comparative study on hot carrier effects in inversion-mode and junctionless MuGFETs," Solid-State Electronics, vol. 79, pp. 253-257, Jan. 2013.

[14] C-H Park, *et al*., "Investigation on Hot Carrier Effects in n-type Short-Channel Junctionless Nanowire Transistors," Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on, Birmingham, UK, 20-23 Aug. 2012.

[15] C-W. Lee, *et al*., "Junctionless multigate field-effect transistor," Applied Physics Letters, vol. 94, pp. 053511(1-2), Feb. 2009.

[16] J. P. Colinge, *et al.*, "Nanowire transistors without junctions," Nature Nanotechnology, vol. 5, pp. 225–229, Mar. 2010.

[17] C. H. Park, *et al*., "Electrical characteristics of 20-nm junctionless Si nanowire transistors," Solid-State Electronics, vol. 73, pp. 7-10, Jul. 2012.

[18] R. Rios, *et al*., "Comparison of junctionless and conventional trigate transistors with Lg down to 26 nm," IEEE Electron Device Letters, vol. 32, pp. 1170-1172, Sep. 2011.

[19] R. Yu, *et al*., "Junctionless nanowire transistor fabricated with high mobility Ge channel," Physica Status Solidi RRL, vol. 8, pp. 65-68, Oct. 2013.

[20] Y. Kamata, et al., "Superior cut-off characteristics of Lg=40 nm Wfi n=7 nm poly Ge junctionless tri-gate FET for stacked 3D circuits integration," Symposium on VLSI Technology Digest of Technical Papers, T94–T95.

[21] S. Sahay, M. J. Kumar, "Diameter Dependence of Leakage Current in Nanowire Junctionless Field Effect Transistors," IEEE Transactions on Electron Devices, vol. 64, pp. 1330-1335, Mar. 2017.

[22] R. Yu, *et al*., "Impact ionization induced dynamic floating body effect in junctionless transistors," Solid-State Electronics, vol. 90, pp. 28-33, Dec. 2013.

[23] C-W. Lee, *et al.*, "Low subthreshold slope in junctionless multigate transistors," Applied Physics Letters, vol. 96, pp. 102106.1-3, Mar. 2010.

[24] S. M. Sze, "Physics of semiconductor devices," 2nd Ed. New York, J. Wiley & Sons, 1981.

[25] M. Gupta and A. Kranti, "Germanium Junctionless MOSFET with Steep Subthreshold Swing," Electrochemical Society Transactions, vol. 66, pp. 79-86, 2015.

[26] S. Krishnan and J. G. Fossum, "Grasping SOI floating-body effects," IEEE Circuits and Devices Magazine, vol. 14, pp.32-37, Jul. 1998.

[27] M. Gupta and A. Kranti, "Suppressing Single Transistor Latch Effect in Energy Efficient Steep Switching Junctionless MOSFETs," 2017 30th International Conference on VLSI Design and 2017 16th International Conference on Embedded Systems (VLSID), Hyderabad, India, 7-11 Jan. 2017.

[28] M-S. Yeh, *et al.*, "High Performance Ultra-Thin Body (2.4nm) Poly-Si Junctionless Thin Film Transistors with a Trench Structure," 2014 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 15-17 Dec. 2014.

[29] J. P. Colinge, "Silicon-on-insulator (SOI) junctionless transistors, Chapter 6 In Silicon-On-Insulator (SOI) Technology," Woodhead Publishing, pp. 167–194, 2014.

[30] J. P. Colinge, et al., "Junctionless Transistors: Physics and Properties, In Semiconductor-On-Insulator Materials for Nanoelectronics Applications" Springer Berlin Heidelberg, pp. 187-200, 2012.

[31] V. Thirunavukkarasu, et al., "Gate-all-around junctionless silicon transistors with atomically thin nanosheet channel (0.65 nm) and record sub-threshold slope (43 mV/dec)," Applied Physics Letters, vol. 110, pp. 032101.1-5, Jan. 2017.

[32] T-K. Chiang, "A Quasi-Two-Dimensional Threshold Voltage Model for Short-Channel Junctionless Double-Gate MOSFETs," IEEE Transactions on Electron Devices, pp, 2284- 2289, vol. 59, Sep. 2012.

[33] L. Ansari, *et al*., "Simulation of junctionless Si nanowire transistors with 3 nm gate length," Applied Physics Letters, vol. 97, pp. 062105, 2010.

[34] J. P. Colinge, *et al.*, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," Solid-State Electronics, vol. 65-66, pp. 33–37, Nov-Dec. 2011.

[35] G. Leung, "Variability and Heterogeneous Integration of Emerging Device Technologies," PhD dissertation, University of California, Los Angeles, 2015.

[36] A. Asenov, *et al*., "Simulation of statistical variability in nano-CMOS transistors using drift-diffusion, Monte Carlo and non-equilibrium Green's function techniques," Journal of Computational Electronics, vol. 8, pp. 349-373, Oct. 2009.

[37] J. P. Colinge, *et al.*, "Reduced electric field in junctionless transistors," Applied Physics Letters, vol. 96, pp. 073510, Feb. 2010.

[38] C. Jacoboni, C. Canali, G. Ottaviani, A. Alberigi Quaranta, "A review of some charge transport properties of silicon," Solid-State Electronics, vol. 20, pp. 77-89, Feb. 1977.

[39] D. Y. Jeon, "Revisited parameter extraction methodology for electrical characterization of junctionless transistors," Solid-State Electronics, vol. 90, pp. 86-93, Dec. 2013.

[40] K-I. Goto, *et al*., "Mobility and screening effect in heavily doped accumulation-mode metal-oxide-semiconductor field-effect transistors," Applied Physics Letters, vol. 101, pp. 073503, Aug. 2012.

[41] T. Rudenko, *et al*., "Electron mobility in heavily doped junctionless nanowire SOI MOSFETs," Microelectronic Engineering, vol. 109, pp. 326-329, Sep. 2013.

[42] M. P. Persson, *et al*., "Charged impurity scattering and mobility in gated silicon nanowires," Physical Review B, vol. 82, pp. 115318, Jun. 2010.

[43] ATLAS User Manual: Device Simulation Software, 2012.

[44] S. Tyaginov, "Physics-Based Modeling of Hot-Carrier Degradation. Chapter in: Hot Carrier Degradation in Semiconductor Devices," Springer International Publishing, 2015.

[45] E. H. Poindexter, P. J. Caplan, B. E. Deal, R. R. Razouk, "Interface states and electron spin resonance centers in thermally oxidized (111) and (100) silicon wafers," Journal of Applied Physics, vol. 52, pp, 879-884, Feb. 1981.

[46] R. Trevisoli, R. Trevisoli Doria, D. Michelly de Souza, M. A. Pavanello, “Extraction of the interface trap density energetic distribution in SOI Junctionless Nanowire Transistors,” Microelectronic Engineering, vol. 147, pp. 23-26, Nov. 2015.

[47] T. Kubota, A. Asano, “Theoretical and spectroscopic studies of gap-states at ultrathin silicon oxide/silicon interfaces,” The Journal of Chemical Physics, vol. 111, pp. 8136-8143, Nov. 1999.

[48] P. M. Lenahan, P. V. Dressendorfer, “Hole traps and trivalent silicon centers in metal/oxide/silicon devices,” Journal of Applied Physics, vol. 55, pp. 3495-3499, May. 1984.

[49] J. P. Campbell, P. M. Lenahan, “Density of states of Pb1 Si/SiO2 interface trap centers,” Applied Physics Letters, vol. 80, pp. 1945-1947. Mar. 2002.

[50] S. Kim, S-J. Choi, D-I. Moon, Y-K. Choi, “An Extraction Method of the Energy Distribution of Interface Traps by an Optically Assisted Charge Pumping Technique,” IEEE Transactions on Electron Devices, vol. 58, pp. 3667-3673, Nov. 2011.

[51] C. Hu, *et al*., “Hot-electron-induced MOSFET degradation – Model, monitor, and improvement,” IEEE Transactions on Electron Devices, vol. 32, pp. 375-385, Feb. 1985.

[52] J. M. Rabaey, A. P. Chandrakasan, B. Nikolić, “Digital integrated circuits : a design perspective,” Pearson Education, 2003.

[53] S. Mookerjea, R. Krishnan, S. Datta, V. Narayanan, “On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors,” IEEE Electron Device Letters, vol. 30, pp. 1102-1104, Oct. 2009.

6. Conclusion

In this thesis, we have presented a contribution to the study, modeling and reliability evaluation of tunnel and junctionless field effect transistors. In the first part, a brief physical description of tunneling mechanism in semiconductors was introduced along with the broadly used semi-classical models, which allowed us to develop a comprehensive study on the use and the control of tunnel transport in transistors. A detailed description of the device working principle was then carried out. Although TFET can achieve good performances, it is still falling short of the actual roadmap requirements. Investigation on practical design reveals some promising leads to overcome the physical limitations. A possible mixing and compromise between these solutions may lead the TFET surpassing the advanced MOSFET performances and being a real alternative for future technology.

The next step was the development of a semi-analytical model of an undoped VSG-TFET that can be used as a core model for TCAD simulators. Basing on the previous physical description and the Kane model, a continuous and accurate tunneling current expressions based on cylindrical harmonics solution of the 2-D potential was elaborated. The proposed model describes remarkably the ambipolar tunneling and dual modulation effects. Good agreement with simulated data at different bias conditions was obtained. The model continuity and large transfer characteristic permitted the evaluation of device scaling capability, analog/RF performance and linearity. The role of introducing a high-κ layer on the gate oxide in improving the VSG-TFET behavior was investigated for high-performance analog/RF applications. It was shown that dimensions and operating supply range should be carefully chosen upon the device application. Globally, the results demonstrate good analog/RF performances, a comfortable upper limit of the dynamic operating range with a high gain and an acceptable cut-off frequency making of TFET structure a promising candidate for low power analog/RF applications.

As local tunneling models are not applicable to heterostructures, a new semi-analytical model of an undoped heterojunction VSG-TFET based on nonlocal approach was developed. Using the previously elaborated solution of the channel 2-D potential, a consistent exponential approximation valid for long channels was adopted. Expressions of the junctions' potential were derived based on both Fermi-Dirac and Boltzmann statistics to

take into account the extensions degeneracy. Using conformal representation technique, suitable expressions of the source and drain extensions surface potential that take into account the fringing field were developed. The heterostructure band alignment was computed using the affinity rule. The exponential potential profile over the whole device allowed the analytical integration of the tunneling probability basing on the WKB approximation. Reasonable estimation of the tunneling current was obtained by an appropriate set of the wavevectors and region contribution. The model was validated and calibrated with 2-D numerical simulations. The demonstrated validity of the model for a wide range of device material definitions, dimensions and supplies permitted to gain insight on the heterojunction TFET physics as well as the impact of the possible band alignment types and source doping. Analytical terminals capacitance model was also derived. Multi objective genetic algorithms optimization was carried out. It permitted to outline new design rules for digital and analog applications depending on the targeted performance.

In the final chapter, the primordial JLFET reliability issue at nanoscale domain was investigated. A comparative study of the hot carrier effect on JL and IM VSG-MOSFET was carried out. The analysis focused on the interface state creation and the subsequent impact on the devices performances. Numerical simulation of both devices degradation in time domain revealed a particular distribution of the interface states for each device type. Reproducing the interface traps profile evolution and incorporating the amphoteric property of the states, a more realistic behavior of these latter was obtained. The numerical investigation demonstrates relative good immunity of the JL device against HCD. For longer aging phenomenon, this immunity results in superior electrical performance relatively to the IM device. Identical behavior of the HCD was obtained for shorter gate length with a sensible reliability improvement. A better immunity of JL based CMOS inverter was also observed in both static and dynamic operation. The study permitted the elucidation of the enhanced JLFET reliability and lifetime in a more insightful manner that will facilitate the development of new models accounting for HCD.

Future works and perspectives

The successful development of the VSG-TFET model represents a first step in the elaboration of a complete compact model. To this aim, additional physical models should be included such as:

- the channel transport limitation on the tunneling current by developing a new expression of the drain modulation that incorporates the channel mobility;
- the Fermi levels difference between the two sides of tunneling junction in order to satisfy the zero bias condition;
- the source/drain degeneracy and Fermi distribution impact on the tunneling current describing a more complete effect of the doping concentration;
- the depletion and fringing effect on the SDEs with accurate and simple expressions that preserve the current model continuity;
- the terminals capacitance model to complete the core model;
- the TAT and SRH generation which are dominant for low gate bias.

The enumerated steps in the completion of the core model will reduce the number of fitting parameters or give a physical meaning to these latter. Nevertheless, a pure analytic model will be impossible to obtain owing to the nature of the assumptions used as core foundation either in the Kane or the VSG-TFET model. It is also important to keep and valorize the advantage of the model continuity and large domain of validity.

The second developed model for heterostructure TFETs yields encouraging results but present a non-negligible lack of accuracy. Moreover, essential transport mechanisms involved in subthreshold regime such as TAT and SRH generation are not considered. The inclusion of these models would be another step in the completion and refinement of the core model along with the incorporation of additional physical models such as:

- the channel transport limitation on the tunneling current by developing a new expression of the drain modulation that incorporates the channel mobility;
- the incorporation of the charge dipole creation effect on the electrostatic distribution;

- the development of physical based expression to evaluate the branch point;
- the gate underlap and overlap over the extensions as it is rarely aligned with the junctions in practice;
- the lattice mismatch consideration to avoid high defective interface;
- the adaption of the model for shorter channel lengths;
- the direct and TAT from the source to the drain for lengths below 20 nm.

The enumerated propositions will finalize the development of a fully functional and accurate compact model. Nevertheless, and as for many compact models and commercial tools, the use of calibration parameters will be indispensable. The enlargement of the model to other multigate structures is also practicable. The advantage of ultra-thin TFETs should be exploited in this case and the quantum confinement must then be taken into account.

The reliability evaluation of the JLFET was performed by considering only HEI on the creation of interface traps. In order to develop a robust model of interface traps distribution and evolution in JL devices, it is essential to enlarge the study and consider other degradation mechanisms, models and parameters such as:

- the channel hot electron contribution on interface traps creation;
- the effect of concomitant oxide trapping/detrapping and fixed oxide charge;
- the energy driven approach and bias temperature instability degradation in order to gain a larger and complete picture of the device aging process;
- different insulator and substrate materials, channel doping and device dimensions, especially ultra-thin body structures;
- AC stress impact on the interface states distribution.

The final aim of the aforesaid propositions is to develop an explicit interface traps distribution model that allows sidestepping the differential equation that describes the traps density evolution in both time and space domains. In addition to specific energetic distribution, the model could be introduced in the 2-D potential solution of the JL device. The current expression will consequently include the effect of interface traps in a more

physical and realist manner. Such approach will simplify the device reliability assessment at circuit level in much larger integration than the actual commercial tools are able to evaluate.